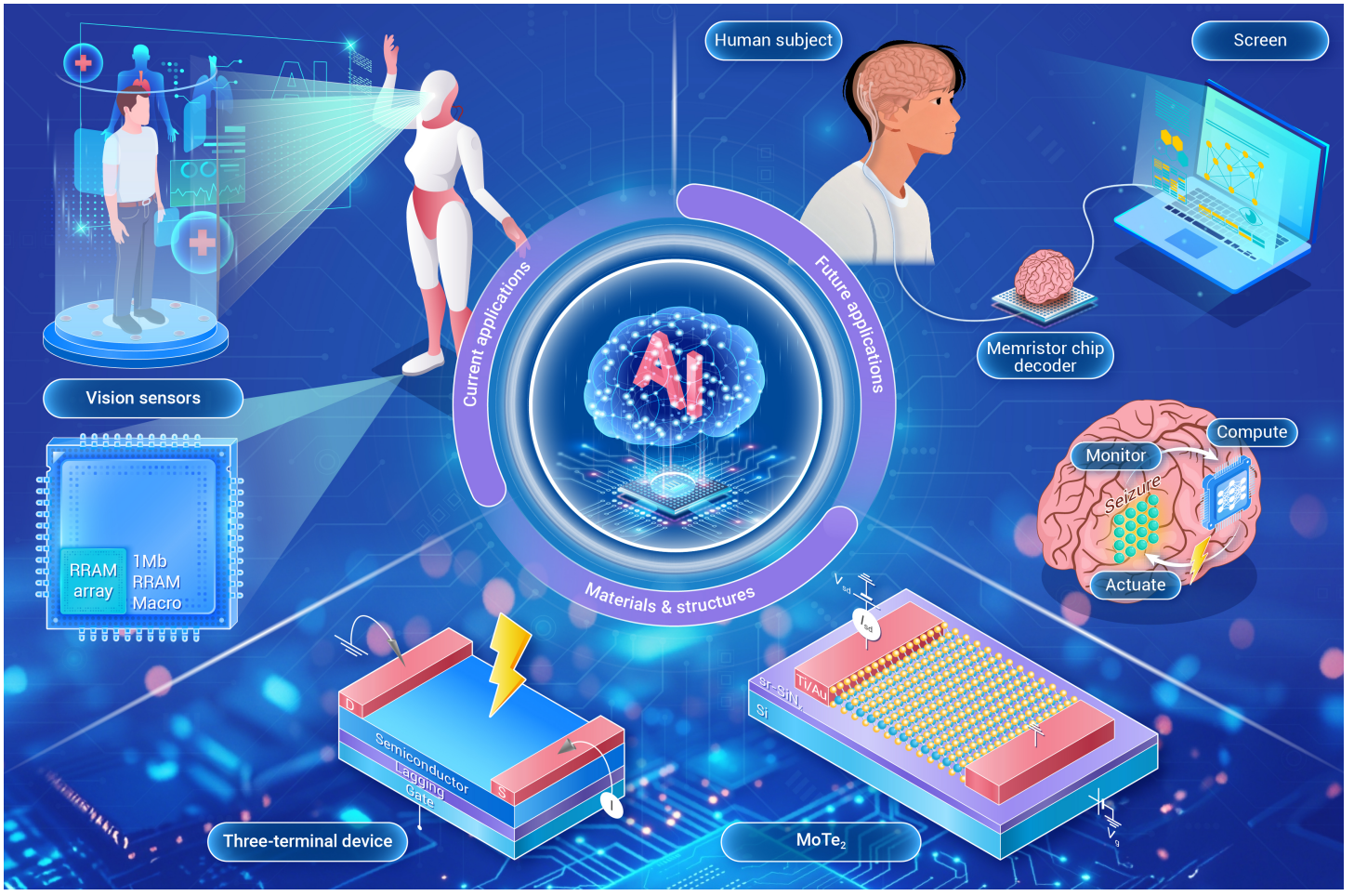
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Recent progress on integrated neuromorphic chips

Xiushuo Gu,[1,7] Lifeng Bian,[1,7] Linrui Cheng,[2,3] Chaoyun Song,[4,*] Yibin Wang,[5] Jianya Zhang,[5,*] and Yukun Zhao[2,3,6,*]
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GRAPHICAL ABSTRACT



PUBLIC SUMMARY

- This review overviews integrated neuromorphic chips based on artificial synaptic devices.
- It summarizes recent advances in synaptic materials, device structures, and chip integration.
- Key progresses in large-scale integration, low power operation, and synaptic plasticity are highlighted.
- Future opportunities of neuromorphic chips in AI, sensing, and intelligent robotics are discussed.

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Semiconductor Devices REVIEW

The Innovation Informatics

Recent progress on integrated neuromorphic chips

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In the post-Moore era, advancing integrated circuits necessitates the development of artificial synaptic devices capable of replicating the functions of human brain with neuromorphic computing, which consists of numerous biological synapses. The neuromorphic chips based on integrated synaptic devices are the promising candidates due to their unique properties, which enable the simulation of human brain and biological synapse plasticity. In recent years, significant progress has been made in the development of optoelectronic synaptic devices and integrated neuromorphic chips. This review summarizes the recent advancements in the integrated synaptic devices, focusing on the structures, integrated technologies and their applications of neuromorphic chips. It discusses the two-terminal and three-terminal configurations of synaptic devices, emphasizing their advantages in simulating biological synapse functions. These advantages include a simple structure, low power consumption, high stability, a wide switching ratio and fast programming speed. Furthermore, the discussion covers the key applications of synaptic devices and integrated neuromorphic chips, such as image recognition, brain-like computing, tactile and vision sensors. For the synaptic-device-based neural networks in image recognition, they have great potential in tactile technology and visual bionics. Other potential applications have also been reviewed and discussed, including intelligent robots, electric skin, human-computer interaction and brain-computer interface, *etc*. Hence, neuromorphic chips have great promising application prospects, which can significantly promote the development of artificial intelligence and human civilization.

INTRODUCTION

The classic von Neumann architecture, with physical separations between storage and processing units, requires frequent data transfers between the processor and memory.[1] This dependency increases power consumption and reduces computing speed, posing significant challenges for applications in emerging fields like the Internet of Things (IoT) and Artificial Intelligence (AI).[2,3] As a result, there is growing interest in using memristor-based neuromorphic computing to overcome the von Neumann bottleneck. The complexity and multifunctionality of the human brain depend largely on neurons and synapses. Synapses play a critical role in transmitting signals from one neuron to another by action potentials.[4,5] The human brain, with approximately 10^{11} neurons and 10^{15} synapses,[6] houses a sophisticated neural network that enables complex neural activities. Recreating the biological functions of synapses is crucial for advancing neuromorphic applications.[7] Memristors, also known as artificial synaptic devices, represent a significant advancement in this context. They efficiently mimic the parallel processing capabilities of the brain, enhancing computational efficacy and performance in neuromorphic systems. This capability is enabled by their real-time response to optical signals, allowing for rapid information processing and reduced data transmission delays and energy consumption.[8] Furthermore, memristors have the potential to unify data storage and processing at the device level, leading to more efficient and compact neuromorphic systems.[9-11]

The integration of components on a single chip is crucial for achieving the accelerated neuromorphic computation.[12,13] The integration of synaptic devices enhances both integration density and energy efficiency in neuromorphic computing chips.[14] Integration density is a key metric for evaluating chip space utilization. The implementation of memristor-based synaptic circuits has the potential to significantly enhance integration density while reducing chip area.[15] These devices also exhibit minimal power consumption, further improving the overall energy efficiency of neuromorphic chips.[16] The integration of synaptic devices also supports high performance and scalability in neuromorphic chips.[17] Large-scale integration of synaptic arrays enables highly parallel analog matrix-vector multiplication, improving computational performance and throughput.[18] Their scalability opens up new possibilities for the development and application of neuromorphic chips.[19] Furthermore, incorporating synaptic devices enables the simulation and modeling of biological nervous systems through neuromorphic chips.[20] These devices can mimic essential neuronal functions, such as all-or-nothing pulse firing, signal amplification and periodic pulsing, enabling a more accurate representation of the biological principles behind neuromorphic computing.[21]

Integrated synaptic devices offer a promising prospect for revolutionizing artificial neural networks, which are crucial for efficiently handling large datasets.[22] These datasets are essential for training complex deep learning models.[23] Compared to conventional hardware, these devices offer significant advantages in energy efficiency and power consumption, allowing for handling larger data volumes while reducing energy consumption.[24] Moreover, the ability of synaptic devices to mimic the plasticity of biological synapses offers an exciting opportunity to enhance adaptive learning and memory. This feature allows artificial neural networks to be more adaptable and responsive when dealing with complex tasks, such as image recognition and natural language processing. Consequently, integrating synaptic devices into neural network architectures could lead to significant advancements in performance and efficiency across various applications.[25,26] The field of AI also benefits from the accelerated development of intelligent systems, improving learning capabilities and enabling real-time data analysis. By employing synaptic devices, researchers can develop more advanced and efficient AI systems that replicate human thought processes, enabling them to perform complex decision-making and reasoning tasks. This has significant implications across fields such as finance, healthcare and transportation.[27,28]

Moreover, the integrated synaptic devices enable more efficient learning mechanisms, which are crucial for advancing self-learning AI systems.[29] These systems can learn and adapt in various environments through continuous adjustment and optimization of their synaptic connections, improving the overall intelligence.[25,30] Furthermore, integrated synaptic devices can process data rapidly, making them suitable for real-time data analysis. This is particularly crucial in domains requiring swift response and decision-making, such as financial trading and intelligent monitoring, as it can significantly enhance system responsiveness and precision.[24] In conclusion, the potential applications of integrated synaptic devices in artificial neural networks and AI are vast and far-reaching. By mimicking the functionality of biological nervous systems, the neuromorphic chips integrated of many synaptic devices not only enhance data processing and learning efficiency but also open new avenues for developing more intelligent AI systems.

This review focuses on the brain-like synaptic devices and the integrated

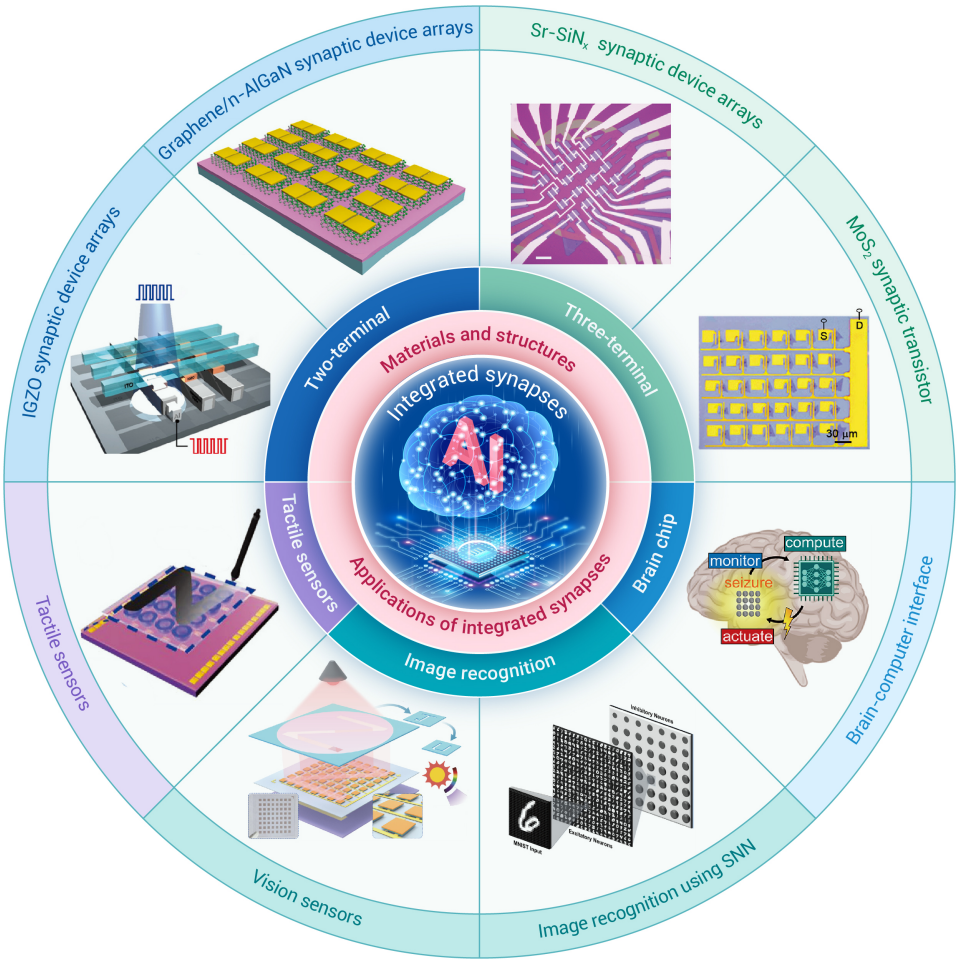


Figure 1. The schematic diagram of materials, structures and applications of neuromorphic chips discussed in this review Reproduced with permission.[31-38] Copyright 2024, Wiley - VCH. Copyright 2020, Elsevier. Copyright 2021, American Chemical Society. Copyright 2023, Wiley - VCH. Copyright 2023, Elsevier. Copyright 2020, Wiley - VCH. Copyright 2024, American Chemical Society. Copyright 2022, American Chemical Society.

technologies for neuromorphic chips, providing a brief historical overview of their development and performance metrics. The discussion covers the materials and structures used in the single device and integrated chips. Finally, the discussion includes the applications of integrated neuromorphic devices. The key elements of this review are schematically illustrated in Figure 1. This review thus offers a brief overview of the current challenges and future prospects for the applications of the basic synaptic devices and integrated neuromorphic chips.

MEMRISTOR BASICS

Principle and characteristic of memristor

As a representative of new brain-like devices, memristor was proposed as a theoretical model as early as 1971, and it was first experimentally verified by Hewlett-Packard Labs in 2008, marking the beginning of an extensive research period in both industry and academia.[39] Similarly, like other passive circuit elements (resistance, capacitance and inductance), the memristor can be derived by relating the four fundamental electrical variables (charge, voltage, current and magnetic flux) to one another. This relationship is expressed by Equation (1):[40]

$$M(q) = \frac{d\varphi}{dq} = \frac{v(t)}{i(t)}. \quad (1)$$

Rapid advancements of the brain at both macroscopic and microscopic levels have significantly improved our knowledge of its operations, thereby influencing the development of bionic computing systems. Research shows that all human perceptual, emotional, learning, forgetting and memory processes are controlled by a complex neural network of neurons and synapses. Neurons are essential for generating and transmitting action potentials within this network.[41] As shown in Figure 2A, a synapse serves as a specialized connection enabling communication among neurons or among the neurons with other cells, such as muscle or glandular cells. This junction consists of a presynaptic membrane (the axon terminal of one neuron) and a postsynaptic membrane (the dendrites or cytoplasm of another neuron), with a synaptic gap in between.[42] A voltage-dependent release of calcium ions (Ca^{2+}) is triggered by a specific change in action potential at the presynaptic membrane, across the synaptic gap. These ions are bound to receptors on the postsynaptic membrane, causing the opening of channels that allow ions to flow.[43] The influxes of permeable ions such as sodium (Na^{+}) or potassium (K^{+}) lead to depolarization of the postsynaptic membrane, known as postsynaptic excitation. Conversely, hyperpolarization of the postsynaptic membrane, caused by the efflux of ions like chloride (Cl^{-}), is called postsynaptic inhibition. The balance between these two mechanisms is crucial for the proper functioning of the entire neural network,[44] which relies on the delicate balance between postsynaptic excitation and inhibition.

The structure of memory processes, especially memristor, closely mirrors synaptic architecture.[45] In analogy with double-terminal (or three-terminal) devices, the top and bottom electrodes (source and drain electrodes) represent the presynaptic and postsynaptic membranes, respectively (Figures 2B & C). In this framework, the light or electrical pulses serve as presynaptic action potentials affecting the synapse. The material between the electrodes mimics a neurotransmitter.[46] Furthermore, modulating the conductance of this active material via optical or electrical stimulation can generate either an excitatory postsynaptic current (EPSC) or an inhibitory postsynaptic current (IPSC). This analogy highlights the potential of synaptic devices to replicate the intricate signaling processes of brain, paving the way for the advancements in neuromorphic computing.[47]

Classification of memristor synapses

Memristor synapses can be classified based on several criteria, including their operating mechanisms and structural configurations, which are also known as synaptic devices. For example, based on their operating mechanisms, synaptic devices can be classified into ionic migration-driven devices (activated by electrical pulses),[48] ferroelectric-based devices (activated by electrical pulses),[49] phase-transition-based devices (activated by electrical and optical pulses),[50] charge trapping and release devices (activated by electrical and optical pulses),[51] and redox mechanism-based devices.[52] These devices utilize materials such as metal oxides, semiconductors, phase-change materials and chalcogenides. Structurally, synaptic devices are be divided into two-terminal devices and transistor-based devices. In these devices, electrodes function as neuron-like components, connecting to the synapse or providing signal stimulation. Two-terminal synaptic devices offer advantages in integration, while transistor-based devices enable precise modulation of electrical behavior via gate voltage control. Synaptic devices are further categorized based on their stimulation type. The main classifications include electrically stimulated and optically stimulated synaptic devices. Recently, optoelectronic synergistic synaptic devices, integrating both electrical and optical stimulation, have gained significant attention for their ability to

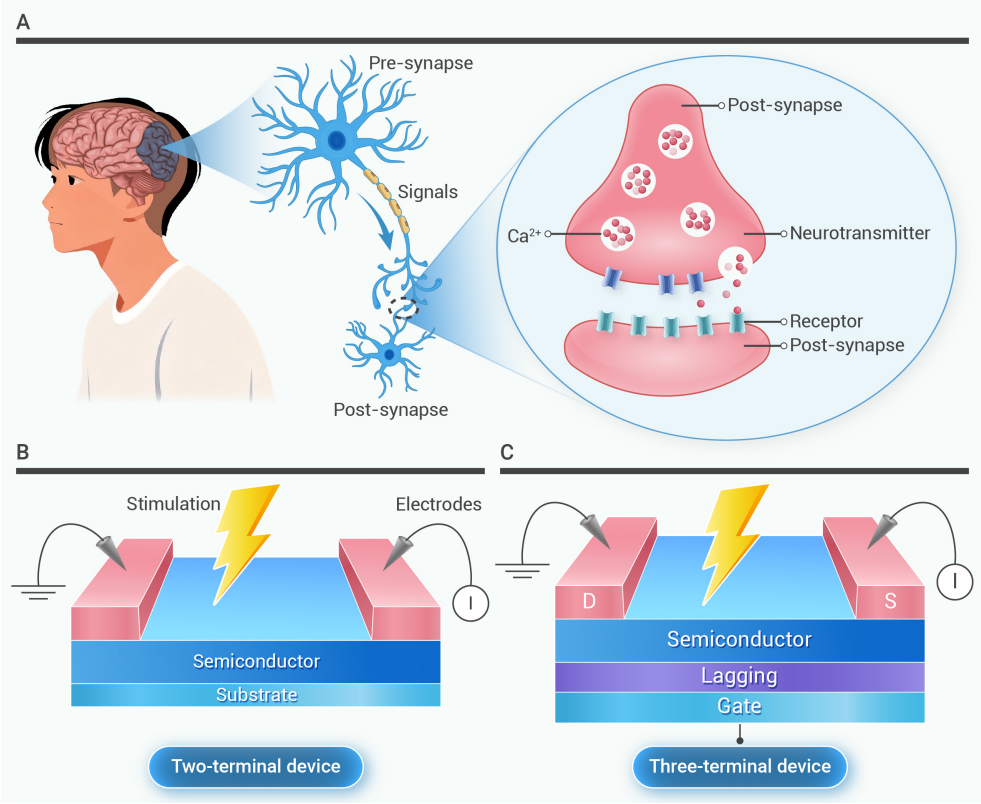


Figure 2. Schematic illustration of biological synapses and artificial synaptic devices (A) A schematic diagram illustrating the structure of a biological synapse. A schematic diagram illustrates the structure of the artificial synaptic devices with (B) two terminals, and (C) three terminals.

coordinate responses to multimodal inputs.

Electrically stimulated synaptic devices replicate biological synaptic plasticity by adjusting their conductivity through electrical pulse signals. The operating mechanism of these devices primarily involves physical processes such as ion migration, ferroelectric effects, phase transitions, carrier trapping and release.[53] The ion migration mechanism entails the movement of metal ions or oxygen vacancies under an applied electric field, forming or disrupting conductive channels, thus altering the resistive state of devices (Figure 3A).[54] The ferroelectric effect utilizes the polarization phenomenon in ferroelectric materials, induced by an electric field, to regulate the electrical performance via precise control of the polarization state.[53] In contrast, the phase transition mechanism induces the changes in the resistive state through material transitions between distinct phases, such as from amorphous to crystalline states. Meanwhile, the carrier trapping and release mechanism modulate the conductivity by altering the carrier concentration through trapping and releasing processes.[55] These electrically stimulated devices offer great potential for the applications in pattern recognition, logic operations, associative learning and filtering.

Optically stimulated synaptic devices use the light signals to emulate biological synapse functions, dynamically modulating conductivity through light pulses or continuous illumination to adjust synaptic weights. These devices offer advantages such as high bandwidth, fast propagation speeds, and resistance to crosstalk, making them highly promising for brain-inspired and neuromorphic computing applications. The operational mechanisms of photo-stimulated synaptic devices primarily include ionization and deionization of oxygen vacancies, carrier trapping and release, and photo-induced phase transitions (Figures 3B–D). The ionization and deionization of oxygen vacancies mechanism is triggered by photo stimulation, resulting in the ionization of oxygen vacancies with the electrons contributing to the conductivity of materials (Figure 3B).[56] The carrier trapping and release mechanism involve the capture of photogenerated carriers by the localized traps within the material (Figure 3C), causing a slow decay of the photocurrent.[57] Meanwhile, the photo-induced phase transition mechanism uses light pulses to induce phase transitions in the material (Figure 3D), altering both its conductivity and light absorption properties.[58] While optically stimulated synaptic devices show significant potential in pattern recognition, logic operations, associative learning and filtering, the substantial improvements are still needed in energy efficiency, linearity, dynamic range, and device retention and durability.

Optoelectronic synergistic synaptic devices combine electrical and optical signals to dynamically regulate synaptic weights, leveraging the complementary advantages of both modalities. By synergistically modulating the conductivity with both electrical and optical inputs, these devices efficiently simulate synaptic functions with low energy consumption. The primary operating mechanisms of these devices include electrically assisted photo stimulation and optically assisted electrical stimulation (Figure 3E). Using subsequent electrical stimulation, electrically assisted photo stimulation achieves inhibitory synaptic functions by erasing carrier trapping induced by photo stimulation.[59] Conversely, optically assisted electrical stimulation reduces energy consumption by modulating ion migration or vacancy formation induced by electrical signals via photostimulation.[60] These devices show significant promise in pattern recognition, logic operations, associative learning and filtering.

While the aforementioned mechanisms effectively emulate synaptic weight updates, their distinct physical principles entail specific performance trade-offs that dictate their suitability for different neuromorphic computing scenarios. First, the devices based on ion migration offer significant advantages in terms of structural simplicity and high on/off switching ratios. However, the inherent stochasticity of ion motion and filament growth often results in substantial variability, posing challenges for high-precision computing.[39] In contrast, ferroelectric devices, driven by electric-field-induced polarization switching, feature nanosecond-scale operation speeds, ultra-low power consumption and superior endurance. Nevertheless, they are often limited by relatively small on/off ratios and retention issues arising from depolarization fields.[61] Phase-transition mechanisms benefit from high technological maturity, multi-level cell capability, and excellent scalability. However, the thermally driven switching process leads to relatively high-power consumption, and the resistance drift inherent to the amorphous state can degrade the temporal stability of synaptic weights.[27] Finally, charge trapping and release mechanisms leverage mature CMOS compatibility and excellent analog state retention, though the high-voltage tunneling process may limit the energy efficiency. Notably, this mechanism serves as the fundamental basis for the majority of optoelectronic synaptic devices, where charge trapping centers are utilized to sustain photogenerated carriers and mimic persistent photoconductivity (PPC) behaviors for in-sensor computing.[62,63] Hence, future research must carefully balance these trade-offs, selecting the most appropriate mechanism tailored to the specific requirements of the target neuromorphic application.

Performance criteria of memristor

The performance criteria are defined related to switching ratio, stability, and linearity for various applications.[64] The switching ratio of a memristor is a key performance indicator for neuromorphic chip applications. The ratio is defined as the resistance of the memristor in the low-resistance state (LRS) relative to that in the high-resistance state (HRS).[65] This is crucial for modeling biological synapses, as it directly affects the dynamic range of weights and representation accuracy. The switching ratio determines the range of weights a memristor can represent. A higher switching ratio enables more precise resistance changes between the LRS and HRS, which in turn improves the accuracy of synaptic weight simulations and the representa-

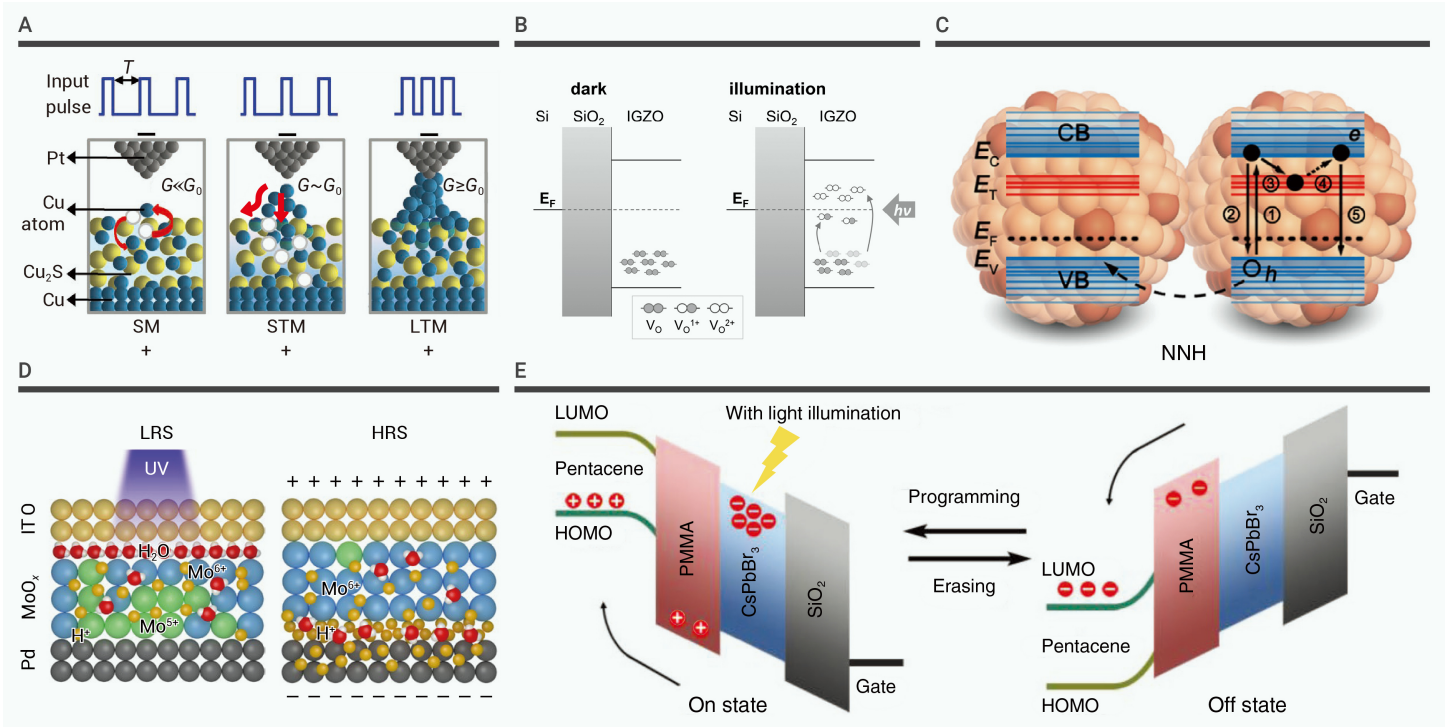


Figure 3. Energy band diagrams illustrating the mechanisms of various types of synaptic device (A) Ion mobility-based mechanisms. Reproduced with permission.[54] Copyright 2017, The Authors, distributed under CC BY 4.0. (B) Ionization and deionization of oxygen vacancies. Reproduced with permission.[56] Copyright 2017, WILEY - VCH. (C) Carrier trapping and release. Reproduced with permission.[57] Copyright 2018, Elsevier. (D) Photoinduced phase transitions. Reproduced with permission.[58] Copyright 2019, Springer Nature. (E) Electrically assisted photo stimulation. Reproduced with permission.[59] Copyright 2018, WILEY - VCH. Reproduced with permission.[60] Copyright 2018, WILEY - VCH.

tiveness of neural network models. In neuromorphic computing, the switching ratio of a memristor plays a key role in determining the dynamic range of a neural network during learning and memory. A larger switching ratio allows for more discrete weight levels, enhancing the ability of neural network to process complex tasks.[66] The switching ratio depends on the electrical properties of the memristor materials. The resistance switching characteristics depend on the combination of materials used, including metal oxides, sulfides or organic materials. Additionally, the physical structure of the memristor, including electrode design and functional layer thickness, affects the switching ratio. Optimizing this structure improves the resistance switching capability. Additionally, fabrication parameters, such as annealing temperature and film deposition conditions, affect the electrical performance of the memristor.[67] Therefore, optimizing material selection, structural design, and manufacturing processes is essential to ensure high switching ratios and meet other key performance criteria for neuromorphic computing.

Memristor stability, defined as the ability to maintain its resistive state over long periods or after numerous switching cycles, is a key indicator of its reliability for neuromorphic chip. In neuromorphic computing, memristors must withstand hundreds of thousands, or even millions, of weight updates without performance degradation.[68] This stability includes resistance to drift, voltage fluctuations and temperature variations, ensuring the memristor maintains accurate weight representation in neural synapse simulations. It ensures computational accuracy in the neural network model and long-term consistency in the learning effect. The memristor stability is strongly influenced by material properties, device structure and fabrication processes. Therefore, careful material selection, structural design optimization, and rigorous production control are essential for achieving high stability in design.[69] Additionally, the memristor's reliability is validated through accelerated aging tests and long-term operational assessments simulating real-world challenges. This testing evaluates its reliability over the expected lifetime.[70] Developing highly stable memristors is crucial for improving the efficiency and cost-effectiveness of neuromorphic computing systems. These devices significantly reduce maintenance frequency and costs while ensuring stable computational performance.

The linearity of a memristor is a key performance indicator for emulating synaptic functionality in neuromorphic computing applications. It is defined as the degree to which changes in memristor resistance correspond to variations in the input signal, directly affecting the precision of neural network models and data processing accuracy.[71] Ideal linearity is characterized by a change in memristor resistance that is perfectly linear relative to the applied voltage or current. This property is vital for implementing the complex neural network algorithms and improving computational performance, as it enables predictable and controllable weight adjustments.[72] However, memristor linearity is influenced by several factors in practical applications, including material properties, device microstructure and fabrication precision. These factors collectively determine the synaptic behavior of the memristor under various operational conditions.[73] Despite challenges, achieving high linearity in the memristor is crucial for advancing neuromorphic computing technology. It can enhance the computational efficiency and broadens the scope of neural network applications, enabling more accurate simulations of human brain function and complex information processing.[74]

Table 1 presents a quantitative summary of several key performance metrics for state-of-the-art memristive devices reported between 2023 and 2025. Recent research utilizing diverse material systems has achieved significant breakthroughs, ranging from emerging 2D transition metal dichalcogenides and halide perovskites to CMOS-integrated oxides. These studies demonstrate remarkable progress in optimizing the trade-offs between switching ratio, long-term stability and weight update linearity, thereby providing robust hardware foundations for high-precision and energy-efficient neuromorphic computing.

In summary, the diverse operating mechanisms of memristors, ranging from ion migration and ferroelectric polarization to charge trapping, provide the fundamental synaptic plasticity required for neuromorphic computing. Each mechanism offers distinct trade-offs in terms of switching speed, energy efficiency and linearity. Understanding these physical principles is crucial for guiding the selection of appropriate material systems and the design of optimal device architectures. In the following section, we will explore how these mechanisms are physically implemented in various materials (e.g., oxides, 2D materials) and structural configurations (two-terminal vs. multi-terminal) to realize high-performance artificial synapses.

Table 1. Key performance indicators of integrated neural chips.

Materials	Switching Ratio (On/Off)	Stability	Linearity	Ref.
PEA_2PbBr_4	10^4	10^4 s	Excellent	23
Pd/TiOx/ZnO/TiN	10^8	10^4 s	Excellent	63
$Pt/HfO_2/Ta_2O_5/TiN$	10^3	10^3 cycles	Excellent	17
$Ta/HfO_2/Pt$	10^6	10^9 cycles	Excellent	16
2D MXene ($Ti_3C_2T_x$)	10^2	10^4 s	Excellent	18
Ga_2O_3/MoS_2	10^2	10^3 s	Excellent	75
s-SWCNTs	10^5	10^3 cycles	Excellent	76
HfO_2/Ta	10^3	10^6 cycles	Excellent	16
2D Halide Perovskite	10^4	10^4 cycles	Excellent	23

MATERIALS AND STRUCTURES OF NEUROMORPHIC CHIP

The strengthening or weakening of synaptic connections, particularly changes in synaptic weights, is a critical mechanism in the nervous system.[77] These changes are typically classified as short-term and long-term, corresponding to short-term and long-term synaptic plasticity, respectively. Short-term synaptic plasticity includes short-term potentiation (STP) and short-term depression (STD), while long-term synaptic plasticity involves long-term potentiation (LTP) and long-term depression (LTD). The effects of these processes can last for hours or longer. Other forms of synaptic plasticity also exist, including spike-time-dependent plasticity (STDP), spike-rate-dependent plasticity, spike-amplitude-dependent plasticity and paired-pulse facilitation (PPF).[78,79]

To achieve high-performance neuromorphic computing, the selection of active channel and switching materials is as critical as the device architecture. The devices discussed in this review primarily utilize three categories of material systems: metal oxides, low-dimensional (1D/2D) materials and organic/biomaterials. Metal oxides, such as indium gallium zinc oxide (IGZO)[35] and Ga_2O_3,[75] are widely adopted due to their high stability, mature deposition processes and compatibility with large-scale integration, typically exhibiting reliable resistive switching or channel conductance modulation. In parallel, emerging low-dimensional materials like $MoTe_2$,[33] graphene[32] and MoS_2[34,80] have gained significant attention due to their atomic thinness and dangling-bond-free surfaces, which enable excellent electrostatic control and low-power operation. Notably, the unique planar structure of materials like MoS_2 also facilitates the development of advanced multi-terminal architectures (e.g., four-terminal devices), offering enhanced flexibility in synaptic weight modulation. Furthermore, organic polymers and natural biomaterials, such as P(VDF-TrFE)[36,81] and PVA/lignin composites,[82] offer unique advantages including mechanical flexibility, biocompatibility and solution processability, making them ideal candidates for wearable neuromorphic systems.

Neuromorphic chips integrated by massive artificial neurons and synapses are essential to emulate human brain functionality. Conventional memristors have been extensively studied for their stable performance and mature fabrication processes. However, individual conventional memristors often lack the speed and capacity required for large-scale storage and computation. Neuromorphic devices with traditional oxide materials are quite difficult to perform integration to achieve chip functions.[83-86] These devices are categorized based on the number of terminals, classified as either double-ended or triple-ended devices. The following discussion presents applications of integrated neuromorphic devices using various materials and mechanisms. This summary includes the key characteristics of these devices, such as structural features, switching ratios, retention times and other pertinent details, along with their advantages and potential applications. Categorizing transistors and integrated circuits by their physical composition and structure has facilitated the development of low-power artificial synapses.[62]

Two-terminal neuromorphic memristors

Sung Hyun Jo et al. proposed an early model of bipartite memristor using nanoscale silicon materials.[87] The device includes the complementary metal-oxide-semiconductor (CMOS) neurons and amnesic synapses that support essential synaptic functions, such as timing-dependent plasticity (STDP). The integration of cross-array structures on a single chip result in the formation of double-ended amnesic synapses at each crossing point. These structures enable high-connectivity and high-density interconnections between CMOS-based presynaptic and postsynaptic neurons, providing potential for efficient computation.[87]

In 2021, Seungho Song et al. introduced a solution-processed oxide semiconductor, indium gallium zinc oxide (IGZO), for fabricating optoelectronic synaptic arrays.[31] These synaptic arrays emulate the structural and signal processing characteristics of biological nervous systems, offering advantages in speed, bandwidth, parallel processing and low power consumption. They employ a vertically stacked metal-insulator-semiconductor-metal (MISM) configuration for double-ended devices, with IGZO as the photoactive layer. This design allows the device to emulate synaptic functions by modulating conductance through optical stimulation. A 3×3 IGZO synaptic array exhibits synaptic behavior, a key neural activity in the brain for neural coding and auditory recognition.[31] With light signals received through transparent indium tin oxide (ITO) electrodes at the top and electrical signals through aluminum electrodes at the bottom. Upon exposure to ultraviolet (UV) light, the IGZO synaptic device shows a gradual increase in photocurrent and prolonged current decay, exhibiting characteristics similar to those in biological synapses.[56,88] By modifying the electrical and optical signal parameters, the optical response of the device can be accurately regulated to emulate diverse synaptic functions, including short-term and long-term memory. These properties make IGZO synaptic devices a promising foundation for neuromorphic computing systems.

In addition to the promising potential of single-material double-gate devices, heterostructure memory devices with vertical arrays of heterojunctions based on dissimilar materials also show considerable promise. In 2023, Li et al.[75] introduced a memristor based on a Ga_2O_3/MoS_2 heterojunction, which was designed to simulate brain synapse functionality and constructed an artificial visual system. The device responds to specific electrical signals, emulating various synaptic functions, including short- and long-term plasticity. It also responds to optical signals, enabling transitions from short-term to long-term memory and facilitating the "learning-forgetting-relearning" process. Using its exceptional optical response, a 16×16 optical performance of the memristor (MMOM) array was designed to emulate the sensory-memory integration function of the human visual system. Furthermore, by using both positive and negative electrical signals, a modulated synapse was proposed to demonstrate its ability to simulate visual synaptic functions. The device exhibits a gradual increase in current during illumination, mimicking the learning process in biological neurons. Conversely, the decrease in photocurrent during the dark period reflects the phenomenon of forgetting.[89,90] Luminance variation directly influences learning and memory intensity, with the higher luminance facilitating long-term memory formation. Modulating the duration and frequency of illumination further controls memory strength and the forgetting rate.[91,92] The experimental results show that as illumination duration increased, the device's light current response

and sustained photocurrent grow, indicating a transition from short-term memory (STM) to long-term memory (LTM). The conversion from STM to LTM could also be achieved by adjusting the number of light pulses. The device stability is validated under various continuous light intensities, confirming long-term reliability under intense light and good pulse stability under rapidly changing light conditions. By applying continuous light pulses, the device simulates the learning process in the human brain. The processes of forgetting and relearning are characterized by increasing memory strength with each repetition, resulting in a faster learning rate and slower forgetting rate. These light-induced memory forms resemble those in the visual cortex and provide a crucial foundation for developing artificial vision systems.[93,94]

In 2024, Chen et al. introduced a heterojunction photonic artificial synapse device array based on a graphene/n-AlGaN heterostructure.[32] This array is realized by using a photoresponsivity polymer (PSP) as a solid carbon source for in-situ growth of diamond-like carbon patterns on various substrates. This approach avoids the need for catalytic metal foils, which are required in traditional graphene growth.[95,96] The synapse array can mimic the transient and sustained plasticity of biological synapses by modulating light pulses in frequency, power density and number, as well as spike-dependent plasticity. The array can also emulate the visual learning process in the human brain, facilitating the initial identification and memory formation using light pulses.[61,97] The current-voltage-time (IVT) curves evaluate the response, substantiating the potential of this graphene-based photonic artificial synapse array for simulating biological visual perception.[98]

In 2025, Huang et al. reported a fully integrated optoelectronic memristor (OEM) array for multimodal in-sensor computing.[63] The OEM employs a simple two-terminal metal–semiconductor–metal structure, where both electrical bias and optical illumination regulate conductance states. This compact design enables high-density integration while supporting multifunctional modulation. Leveraging the synergy of electrical and optical stimuli, the device exhibits stable multilevel conductance tuning and reliable long-term potentiation/depression, effectively mimicking synaptic plasticity. Furthermore, the integrated array directly processes complex spatiotemporal signals within the sensor plane, achieving tasks such as image recognition and multimodal learning without external memory. Electrical and optical characterizations confirm its robustness, underscoring the potential of OEM-based two-terminal architectures for bridging perception and computation in neuromorphic systems.

Three-terminal neuromorphic transistors

Signaling and self-learning occur simultaneously within the neural network of the human brain. Although neuromorphic systems with bipartite structures offer advantages, they have limitations in homogeneity and cycle stability.[99-102] Thanks to the gate-driven process, transistor-based neuromorphic devices offer long-term operational stability and high uniformity.[103] In this configuration, the gate of the neuro-electronic field-effect transistor acts as a synapse for the presynaptic neuron, while the channel functions as the postsynaptic neuron. The gate regulates the channel conductivity, enabling simultaneous stimulation and signal reception.[104,105]

Xiang et al. analyzed the memory behavior of Sr-SiN_x field-effect transistors (FETs) incorporating multilayer $MoTe_2$, focusing on the retention, cycling durability, temperature endurance and transistor functionality under electrical stimulation.[33] Figure 4A shows the three-terminal structure of the Sr-SiN_x FET, consisting of a source electrode, drain electrode and gate electrode, which controls current flow between the source and drain. Adjusting the gate voltage (V_g) allows the Sr-SiN_x FET to mimic synaptic plasticity, supporting signal transmission and processing similar to biological neural networks.[106] A positive gate voltage (V_g) stimulates the excitatory postsynaptic current (EPSC), while a negative voltage stimulates the inhibitory postsynaptic current (IPSC).[107] The amplitude and number of V_g pulses can simulate short-term plasticity (STP) and long-term plasticity (LTP). Short-term plasticity requires a single gate pulse, while long-term plasticity needs a series of gate pulses that accumulate in the transistor, reflecting the long-term synaptic weight changes in biological synapses. To enable more complex neural network calculations, a 4×4 Sr-SiN_x FET-based synaptic array is developed to simulate a three-layer artificial neural network (ANN) for pattern recognition.[108] By adopting this approach, Sr-SiN_x FETs have shown their ability to emulate synaptic functionality at the device level and perform complex neural network computations at a larger scale.

Moreover, Huang et al. introduced a multifunctional photonic nanowire array based on a single layer of molybdenum disulfide (MoS_2) using the chemical vapor deposition (CVD) method, capable of mimicking human associative memory (Figure 4B).[34] The work begins by exploring the cognitive capacities of the human brain, derived from the processes like photoreceptor cell phototransduction, synaptic transmission, and visual information preprocessing before the physiological response in brain.[109-111] As artificial intelligence (AI) advances, research is focused on developing synthetic photonic systems that mimic the human retina and brain functions.[112,113] The resulting electronic devices exhibits characteristic photonic circuits and stable optical responses. Laser-triggered photochemical responses, including short-term potentiation (STP), long-term potentiation (LTP) and paired-pulse facilitation (PPF), are recorded under different stimulation wavelengths (450, 532 and 633 nm) and intensities. Figure 4B outlines the device structure, showing how the device generates photocurrent by splitting electron-hole pairs at the MoS_2/SiO_2 interface, followed by carrier transportation and behavior. The performance of MoS_2 transistor devices can be optimized by adjusting excitation wavelengths and increasing pump laser intensity. A 5×6-pixel induction and processing system can emulate the learning, forgetting and associative memory processes in the human brain.[34] The recovery of a 633 nm stimulation record, obscured by deeper memory, marks an advance in brain-like artificial intelligence.[84,114,115]

Zhang et al. reported the creation of a synaptic transistor array using a composite electrolyte film of polyvinyl alcohol (PVA) and lignin.[82] As shown in Figure 4C, the array is a three-terminal device, and the team successfully fabricated a 10×10 crystalline field-effect transistor array using photolithography. Each crystalline silicon device employs a composite PVA/cellulose acetate electrolytic gate dielectric. The synapse functions, including EPSC and PPF, are achieved by applying voltage pulses at the gate. In an EPSC test, applying a series of gate pulses simulates the biological synapse response, showing an increase in postsynaptic current with more pulses. It is similar to long-term potentiation (LTP) in biological synapses.[116,117] PPF testing evaluates short-term synaptic plasticity by measuring the response change between two successive pulses. The response to the second pulse is greater than the first, aligning with the functional characteristics of biological synapses.[118] The array also has the excellent electrical homogeneity, with parameters such as threshold voltage, subthreshold swing, switching ratio and gate leakage current. Regarding energy consumption, a single transistor consumes 0.63 nJ under a 100 ms pulse width, consistent with research on other field-effect transistor (FET) neurons. This suggests that the FET neuron array has potential for various applications, including image processing.[118-120]

Significant progress has been made in increasing the density of synapse-on-chip arrays due to ongoing research efforts. In 2024, Li et al. proposed a high-density artificial synapse array based on uniform electrolyte-gated transistors (EGTs).[121] The array is successfully integrated onto a 2.5×2.5 cm^2 glass substrate using a crossbar structure, achieving a high-density integration of 100×100 EGT units per cubic centimeter. This achievement promotes the development of three-terminal transistor devices for high-density integration.[30,122,123] To resolve the incompatibility between polymer electrolytes and photolithography, the authors introduced a strategy where the dielectric layer was fabricated as the final step, preventing damage to the electrolyte during high-density integration. Furthermore, the introduction of an electrolyte framework, PEO/PVP/LiTFSI/ZIF-67, increased the array conductivity to 2.87×10^{-3} S/cm^2 for improving overall performance.[120,124] However, the development of more efficient peripheral circuits and algorithms for precise control and updating of each synaptic weight is still quite urgent. Success in overcoming this challenge will drive further advancements and practical applications of the three-terminal synaptic device array.[125-127]

Significant progress has been made in emulating neuronal intrinsic plasticity using wafer-scale monolayer MoS_2 devices. In 2025, Wang et al. demonstrated an integrate-and-fire neuron module by coupling a DRAM capacitor with an inverter fabricated on 4-inch monolayer MoS_2 films (Figure 4D).[128] The compact cell, occupying only a few square micrometers, integrates 3 × 3 photoreceptor neuron arrays and achieves a density exceeding 10^4 functional neurons per cm^2. To address membrane-potential drift at scale, a dual-

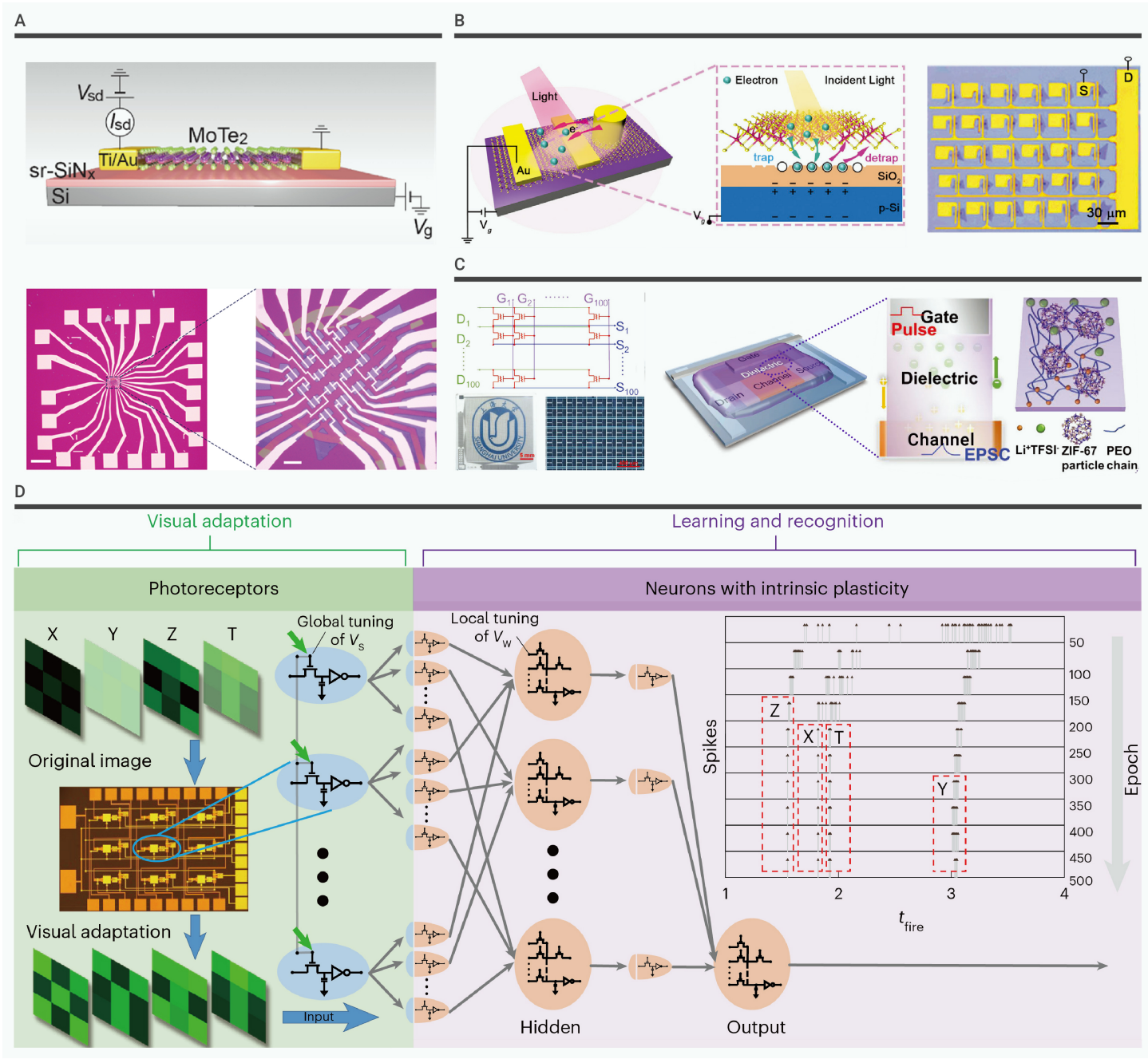


Figure 4. Schematic of the device architecture and working mechanism of a three-terminal artificial synaptic transistor (A) The diagram presents the Sr-SiN_x memory configured as a FET, accompanied by an optical image of the constructed synaptic array that includes electrode pads. A scale bar indicates a measurement of 200 μm. Additionally, an enlarged view of isolated synaptic channels is presented with a scale bar measuring 10 μm, featuring a channel length of 4 μm. Reproduced with permission.[33] Copyright 2021, American Chemical Society. (B) This design incorporates a schematic representation of a MoS_2 synaptic transistor integrated with a gold nanorod functioning under light illumination. A substantial number of plasmonic doping electrons can be injected into the MoS_2 monolayers, enhancing the photocurrent efficiency. An enlarged view illustrates how electrons are trapped or released at the MoS_2/SiO_2 interface, elucidating the operational mechanism of synaptic behaviors. An optical image showing the electrodes arrayed on the MoS_2 monolayers is also included, with a scale bar of 30 μm. Reproduced with permission.[34] Copyright 2023, Wiley - VCH. (C) The illustration features a circuit diagram, a photograph and a micrograph of the array, which is devoid of electrolyte. This setup integrates 100×100 transistors onto a 2.5×2.5 cm^2 glass substrate, with a badge height of 2.5 cm. The diagram depicts the multilayer and lateral architectures of a single unit of the array, along with the multilayer structures associated with the substrate, drain, source pattern, channel, isolation, gate pattern and electrolyte. Furthermore, it elucidates the mechanism of device conductivity modulation and the transportation of Li^+ ions. Reproduced with permission.[121] Copyright 2023, Wiley - VCH. (D) Complete BioNN architecture of the in-situ image processing and STDP learning simulation. Reproduced with permission.[128] Copyright 2025, Springer Nature.

gate strategy is introduced. An access transistor (T_1) enables global reset and leakage tuning, while an independent write line (V_W) locally adjusts the resting potential, thereby realizing intrinsic plasticity without additional synaptic elements. Leveraging the strong photoconductivity of MoS_2, the device supports photopic and scotopic adaptation by tuning light sensitivity via Vs across four orders of incident power. Benchmarking on a biological neural network (BioNN) simulator yielded 92% classification accuracy for four noisy 3 × 3-pixel letters within 300 epochs using time-to-first-spike (TTFS) coding, with an energy cost of only 2.82 nJ per spike—orders of magnitude lower than conventional CMOS neurons. This work highlights the promise of two-dimensional (2D) MoS_2 three-terminal transistors for dense, low-power neuromorphic vision layers.

The pioneering work by Jo et al. has highlighted the potential of dual-terminal memristors based on CMOS for synaptic applications such as spike-timing-dependent plasticity (STDP), offering prospects for high-density integration.[87] Building on this foundation, Song and his team developed photoelectronic synaptic arrays using IGZO materials, effectively emulating the signal processing mechanisms of biological nervous systems.[31] Further

research by Li and colleagues explored multimodal, modulated optoelectronic memristors based on Ga_2O_3/MoS_2 heterojunctions for artificial vision systems, demonstrating learning, forgetting and relearning behaviors. Regarding triple-terminal devices,[75] Du Xiang and colleagues reported the Sr-SiN_x FET,[33] along with the photoelectronic synapses based on MoS_2 monolayers developed by Ming Huang and his team,[34] showcased the ability to modulate synaptic plasticity via gate voltage control. Both teams also achieved complex neuromorphic computations by configuring arrays. Additionally, Zhang et al. reported a synaptic transistor array based on PVA and lignin composite electrolyte films,[82] demonstrating significant progress in simulating biological synaptic behavior, with excellent electrical uniformity and energy efficiency.

Beyond traditional two-terminal and three-terminal architectures, four-terminal devices have emerged as a powerful platform for mimicking complex biological functions, which are often regarded as memory transistors or dual-gate transistors. These multi-terminal structures utilize the planar geometry of 2D materials to integrate non-volatile memory with gate-tunable switching. For instance, Deng et al.[129] reported a linearly programmable memory transistors based on oxygen-doped MoS_2, which successfully emulated hetero-synaptic plasticity through a four-terminal configuration. Expanding on this structural diversity, recent work by Lin et al.[130] demonstrated a versatile dual-gate van der Waals heterostructure transistor. By leveraging a four-terminal architecture, this device not only realized robust neuromodulation but also integrated reconfigurable logic-in-memory operations within a single unit. Such advancements highlight the potential of multi-terminal devices to transcend simple weight storage, enabling the simulation of global regulation and higher-order cognitive processing.

This chapter provides a comprehensive review of recent advancements in neuromorphic devices that replicate brain functions, with a specific focus on dual-terminal and triple-terminal devices, as well as the integration of synaptic device arrays. Some researchers have demonstrated the potential of three-terminal transistor devices for high-density integration, offering valuable insights for future neurocomputing systems.[131] These studies have not only driven breakthroughs at the single-device level but have also introduced innovative approaches for developing efficient neuromorphic computing systems at the array level.

This section has reviewed a wide range of neuromorphic devices based on metal oxides, emerging 2D materials and organic polymers, configured in two-terminal, three-terminal and even multi-terminal architectures. While these individual devices demonstrate promising capabilities for emulating synaptic functions, realizing practical brain-inspired computing requires scaling them up from discrete components into complex and interconnected arrays. Therefore, the next section discusses the critical integrated technologies, including heterogeneous integration, advanced packaging and photonic interconnects. They are essential to assemble these massive device arrays into functional and high-density neuromorphic chips.

INTEGRATED TECHNOLOGY FOR NEUROMORPHIC CHIP

Neuromorphic chips represent a novel computing architecture that mimics the structure and functions of human neural networks, enabling efficient information processing and enhanced learning capabilities.[132] Integration technology plays a crucial role in the evolution of neuromorphic chips.[133] By combining various functional modules and material systems, the chip performance and functional density can be significantly improved, along with its energy efficiency.[134] This chapter will outline several key integration technologies and their applications in neuromorphic chips.

Cross-dimensional heterogeneous integration technology

Cross-dimensional heterogeneous integration technology enables the creation of multifunctional microsystems by integrating devices with varied materials (e.g., silicon, III-V semiconductors, 2D materials), structures and functions on a single chip.[135,136] This technology fully leverages the advantages of diverse materials and devices, overcoming the limitation of using a single material or structure, thereby significantly improving the performance of brain-like chips. Regarding material integration, combining high-mobility III-V family semiconductor materials with silicon-based CMOS technology enhances the performance of neuronal and synaptic devices.[135] For instance, the high electron mobility of III-V materials can enable faster neuron response and lower power consumption. Functional integration, including optoelectronics, RF, sensing and other modules, enables multimodal information processing in brain-like chips.[136] Integrating photonic devices facilitates the rapid transmission and processing of optical signals, improving the chip bandwidth and energy efficiency.[137] In chip design, micro/nano 3D integrated fabrication processes enable multi-layer integration, enhancing integration density and performance.[135]

In recent years, heterogeneous integration technology has the advanced significance in the semiconductor field, particularly in silicon-based optoelectronics and high-speed electronics. Lin et al. developed a method to exfoliate InP thin films from bulk material using sequential He and H ion injection, successfully producing high-quality 2-inch InP-on-Si(100) heterogeneous integrated wafers.[138] The order of He and H ion injection is found to decisively affect InP surface blistering and peeling, while significantly reducing the thermal budget. Similarly, Shi et al. employed an ion-cutting technique to transfer single-crystal GaN films onto CMOS-compatible Si(100) substrates, demonstrating the technique advantages in reducing fabrication costs and enhancing scalability.[139] However, both approaches face challenges, including the impact of residual damage bandwidth on GaN film quality, which remains unresolved. At the transistor level, Wu et al. integrated GaAs pseudo-high electron mobility transistors (pHEMTs) with Si CMOS on the same Si substrate, achieving 5 μm alignment accuracy using wafer bonding.[140] Additionally, Gutierrez-Aitken et al. introduced the diverse accessible heterogeneous integration (DAHI) platform, emphasizing the synergistic integration of multiple materials and technologies.[141] This approach reduces circuit area and offers a reference for future high-performance chip design.

Advanced electronics packaging technology

Advanced electronics packaging technologies provide functions such as signal transmission, power distribution, heat dissipation and mechanical protection by connecting the chip to the external environment. Common packaging technologies include 3D integrated packaging, system-in-package (SiP) and chip-scale packaging (CSP).[135] The application of these technologies in neuromorphic chips can significantly enhance their integration density and performance. 3D integrated packaging technology achieves vertical integration of multi-layer chips using through-silicon via (TSV) technology. For instance, connecting multiple chip layers via TSV enables the creation of more complex neural network structures and increased computing power. SiP and CSP technology integrates various functional modules (e.g., microprocessors, memory, sensors) into a single package.[142,143]

In recent years, as Moore's law and Dennard scaling are invalidity, the semiconductor industry has faced significant challenges in design costs, complexity and performance enhancement. Li et al. proposed a small-chip-based heterogeneous integration technique that combines multiple heterogeneous molds into a single chip via a SIP process.[144] This technique allows molds fabricated at different process nodes to be reused across projects, significantly reducing design costs and improving yields. However, the authors also note that the technology still faces challenges such as the longer design cycles and increased technical complexity. Gambino et al. provided a comprehensive summary of through-silicon vias (TSV) technology,[145] detailing the steps involved in TSV fabrication, such as etching, insulation, metallization, back-end processing, assembly and testing. Although TSV technology has entered the mass production phase, it still faces challenges related to reliability, yield and design complexity. Both studies focus on different aspects of integration technology: Li et al. examine system-level small-chip integration, while Gambino et al. explore the application of TSV technology for hardware connectivity.[144,145] These studies have driven the technological evolution of IC design, but challenges such as cost, reliability and complexity remain to be addressed in practical applications.

Photonic integration technology

Photonic integration technology enables optical signal processing and transmission by integrating components such as waveguides, lasers, modulators and detectors on a single chip. Photonic integration relies on various material systems, including InP-based, silicon photonics (SOI), silicon nitride/silicon dioxide (Si_3N_4/SiO_2), and lithium niobate (LNOI).[146] These material

systems significantly enhance the bandwidth and energy efficiency of neuromorphic chips. InP-based integration technology leverages the high electron mobility and low-loss properties of InP materials for high-speed optical signal processing.[147] For example, InP-based integration enables high-bandwidth optical signal transmission and processing, enhancing the communication capability of neuromorphic chips.[148] Silicon photonic integration (SOI) technology takes advantage of the compatibility with silicon-based CMOS technology, enabling mass production of photonic devices.[149] For example, SOI technology integrates photonic devices with electronic devices, improving the integration density and performance of neuromorphic chips.[150] Si_3N_4/SiO_2 integration (Si_3N_4/SiO_2) technology leverages the low-loss properties of Si_3N_4 and SiO_2 to enable complex passive photonic devices. It enables the creation of low-loss optical waveguides and filters, improving optical signal processing in brain-like chips.[151]

In recent years, photonic integrated circuits (PICs) have made significant progress in communications, sensing and other fields. Hoefler et al. reviewed recent developments in indium phosphide (InP)-based monolithic integrated system-on-chip (SOC) photonic integrated circuits, exploring their potential for extension to foundry services.[148] The research leveraged existing experience in designing and fabricating commercially available coherent optical communication SOCs to develop an optimized, scalable integration platform for a "turnkey" foundry process. Meanwhile, Smit and Williams provided an in-depth analysis of the current status and future trends of InP-based photonic integration platforms,[147] emphasizing the key role of standardized platforms in advancing photonic technologies. InP-based monolithic integration and silicon photonics are the major platform technologies, but the adoption of standardized platforms still faces technical and market challenges. Similarly, Chen et al. reviewed the historical development of silicon photonics,[152] focusing on key milestones such as passive devices, modulators, detectors, light sources and system integration. Silicon photonics have evolved from fundamental research to a revolutionary technology with widespread application potential. Nevertheless, performance optimization and fabrication complexity remain key challenges.

Figure 5 outlines the roadmap for the development of synapse-based devices and neuromorphic chips. Cross-dimensional heterogeneous integration technology will enhance the multifunctionality and performance of neuromorphic chips, allowing them to simulate the complex neural network structure of the human brain more accurately. Advanced electronic packaging technology will improve the integration density and reliability of brain-like chips, expanding their applications in wearable devices, the Internet of Things, and AI systems. Photonic integration technology will offer neuromorphic chips higher bandwidth and lower power consumption, providing a significant advantage in high-speed communication and big data processing. Integration technology is pivotal in the development of neuromorphic chips.

In summary, cross-dimensional heterogeneous integration, advanced electronic packaging technology, and photonic integration technology can significantly improve the performance, functional density, and energy efficiency of neuromorphic chips. These technologies not only leverage the advantages of diverse materials and devices but also overcome the limitations of a single material or structure, enabling more complex neural network structures and enhanced computational capabilities. As these integration technologies continue to evolve, neuromorphic chips are expected to achieve breakthroughs in AI and neuroscience, contributing significantly to the advancement of human society. The development of integration technology will open new possibilities for the future of neuromorphic chips.

APPLICATIONS OF NEUROMORPHIC CHIPS

In the human brain, synapses are the primary means of transmitting and exchanging information, playing a crucial role in learning and information processing.[153-155] In deep learning, synapses facilitate the formation of associations between behaviors and rewards, reinforcing connections between actions and their outcomes. When a behavior is positively reinforced, the corresponding synaptic connections strengthen through a process called synaptic plasticity. This mechanism allows the brain to adapt its decision-making based on past experiences, leading to the development of behaviors that maximize rewards.[156-158] Perception is the process by which an organism interprets information from its environment. It involves the coordinated action of multiple sensory (vision, audition, and touch) systems that convert physical stimuli into electrical signals the brain can process. This complex cognitive activity enables us to construct meaningful models of the external world.

Neural network computing introduces a new approach to the evolution of future computer systems. In contrast to existing computing architectures, neural network computing uses a highly parallel processing approach, employing numerous low-power neurons and synapses to mimic the functionality of human brain.[159-161] This architecture is especially suited for executing vector-matrix multiplication, a key mathematical operation in many AI algorithms and a major technical challenge in AI research and applications. By adjusting the weights of neuron connections, complex data processing and learning tasks can be achieved.[162,163] The following sections will explore various neural network algorithms and their applications in simulating artificial neurons and synapses, mimicking human visual, auditory and tactile processes. These studies support the development of more efficient and intelligent AI systems.

Image recognition

In recent years, the research on bipolar and tripolar integrated circuit devices has advanced significantly. Extensive studies have been conducted in this field. A key application area is image recognition, including handwritten digit recognition and animal classification. In this context, artificial neural networks (ANN) and convolutional neural networks (CNN) have been discussed. This section classifies and summarizes the image recognition capabilities of spike-based neural networks (SNN) with electrocyte synapses, along with a summary of key studies.

Image recognition with ANN. Artificial neural networks (ANNs) are a machine learning technique that emulates biological neural networks, aiming to replicate and understand human cognition. These networks operate through interconnected neurons, each representing a specific output function, known as an activation function. The connections or weights between neurons store information. The output of network depends on the connectivity, weights and activation functions.[162-165] The hardware foundation of ANNs consists of memristor crossbars, which can integrate with external neural networks.[166] Vector-matrix multiplication (VMM) is a core operation closely related to memristor crossbars, using Ohm's and Kirchhoff's laws for summation in a dense crossbar structure. This design improves computational efficiency and offers a novel approach for hardware implementation of ANNs.[167]

Fang et al. developed a photonic synaptic device based on the neural networks of human brain, constructed using an inhomogeneous semiconductor material (NiO/ZnO). This device is used to create a high-density integrated array that simulates short-term plasticity (STP) and long-term potentiation (LTP) in biological synapses. It also allows precise control of synaptic weights using light pulses.[168] This photonic synaptic array is utilized to simulate the supervised learning process of ANNs with the MNIST database of handwritten digits, achieving efficient image recognition. 256 input neurons correspond to 28×28-pixel images of handwritten digits, and 10 output neurons represent digits 0-9. After 1,000 training iterations, the network achieves 77% accuracy even with 40% noise interference, reaching a maximum accuracy of 90.6% in its optimal state. The study also proposes a simplified ANN method that reduces the original network size to 3.78% while maintaining 95% accuracy. It highlights the immense potential of photonic neuromorphic devices in achieving high-performance, fault-tolerant neural network computing.

Dang et al. have proposed a multifunctional 10×10 photonic field-effect transistor (FET) array based on P(VDF-TrFE) and ReS_2.[81] This array is designed to emulate the wavelength selectivity of the human retina and extract target information from noisy environments. The constructed light-electron device array is demonstrated to have the ability to identify, store and preprocess data while also exhibiting exceptional image recognition capabilities. The array uses photoconductive switching to enhance the contrast between the target object and its surroundings while reducing background noise. The accuracy of image recognition after a light pulse stimulus is 72% after 40 periods, indicating that surrounding interference makes it difficult for the network to identify crucial information. However, after preprocessing with a photodiode array, accuracy increased to 100% after 40 periods with 100

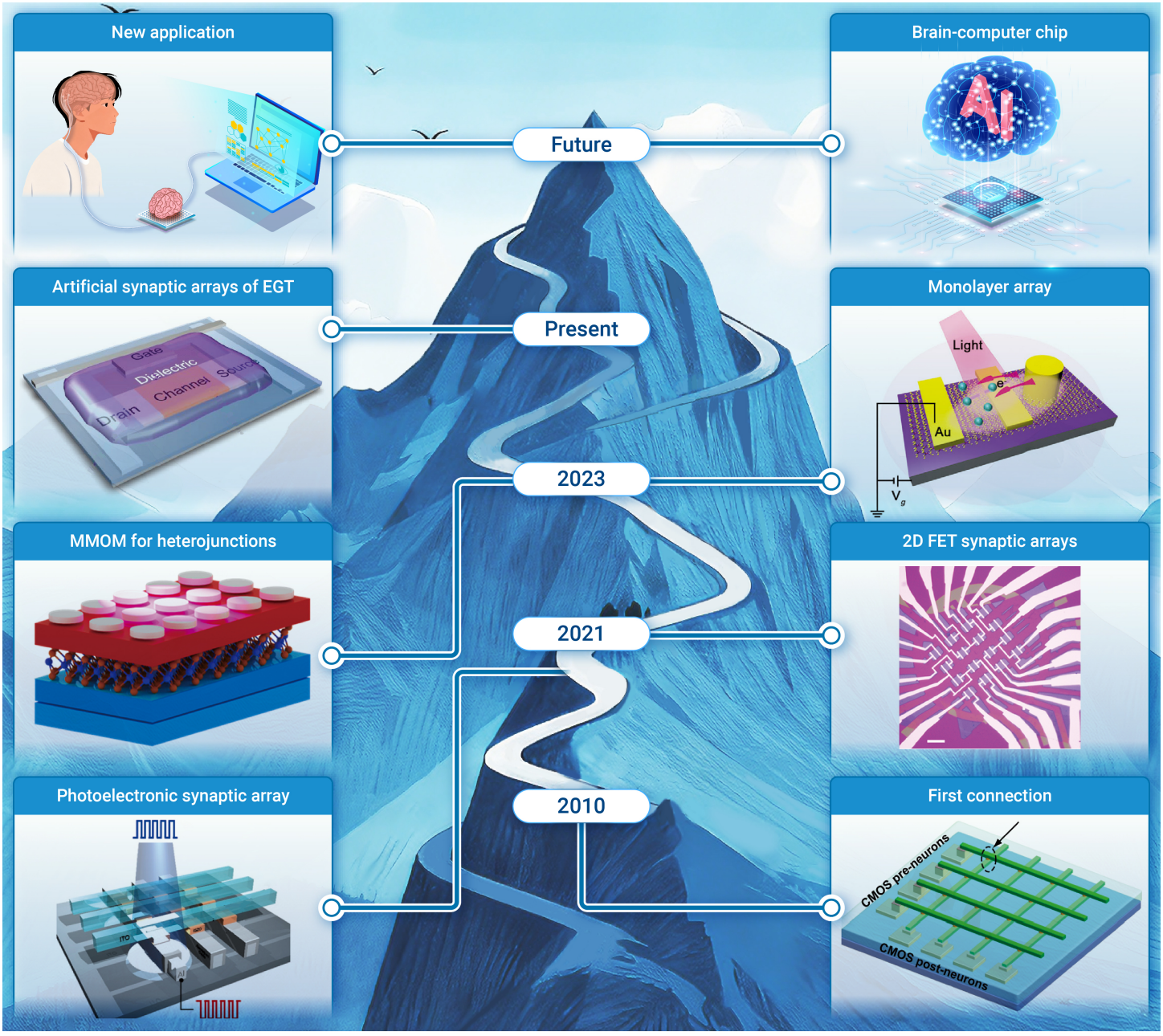


Figure 5. A roadmap outlining the development of integrated synaptic-based chips and identifying the trends for future work Reproduced with permission.[31,33,34,75,80,87,121] Copyright 2010, American Chemical Society. Copyright 2023, Elsevier. Copyright 2021, American Chemical Society. Copyright 2023, Wiley - VCH. Copyright 2023, Wiley - VCH. Copyright 2025, Springer Nature. Copyright 2022, American Chemical Society.

pulses. The recognition rates for 100 pulses and 300 pulses increase significantly to 95% and 96%, respectively. However, the precision level of 95% of 100 pulses is comparable to that of 300 pulses, requiring a significantly shorter duration. The results demonstrate the potential of the developed ferroelectric photonic crystal array for perception, target recognition and energy-efficient processing, laying the foundation for emulating the human visual system and highlighting its extensive applications in future neuromorphic computing and intelligent visual systems.

According to the previous works, the synapse-integrated devices can effectively handle handwritten digit recognition tasks. However, these devices struggle with more complex image recognition tasks, as processing large amounts of data slows their learning efficiency. In contrast, ANNs are robust and fault-tolerant to noise, making them the preferred method for implementing synaptic integrated circuits in image recognition.

Image recognition with CNN. Deep neural networks (DNNs), or deep learning, are a machine learning technique that mimics the structure and function of human neural networks. This method focuses on learning from data through representation, building on the concept of ANNs and evolving from early ANN models. DNNs include various network types, such as convolutional neural networks (CNNs), recurrent neural networks (RNNs), and generative adversarial networks (GANs). These networks show distinct capabilities in image processing, audio analysis, time series data analysis and image generation.[169-172]

A CNN is a type of DNN that uses both a convolutional layer and a pooling layer. CNNs consist of an input layer, convolutional layer, activation function, pooling layer and fully connected (FC) layer. The spatial structure of input data involves the arrangement and connections of components at different levels within the image. For example, in a facial image, spatial features include the arrangement of the eyes, nose and mouth, the distances between these features, and their angles relative to each other.[115,173,174] Naqi et al. developed a transistor array based on IGZO materials to simulate complex neural networks and synaptic functions.[35] The team used this IGZO-based transistor array to simulate multi-level data storage mechanisms, crucial for vector-matrix multiplication. In their CNN simulations, they used the ResNet-

20 model and conducted supervised learning (SL) simulations on the MNIST database. In this simulation, 400 input neurons correspond to 20×20-pixel MNIST images, and 10 output neurons represent digits 0–9. 8,000 images are randomly selected from 60,000 for training and 10,000 for testing to assess identification accuracy. After 125 training iterations, the system achieves a recognition accuracy of 91.1%, close to the ideal neural network accuracy (94.1%). The results demonstrate high identification accuracy and validate the potential of IGZO synaptic arrays in mimicking human brain synapses and performing complex neural computations. These findings offer a promising approach for using synaptic arrays in handwritten character recognition and lay a foundation for developing neural computing systems based on non-volatile memory devices.

Image recognition with SNN. The spiking neural network (SNN), representing the third generation of neural networks, is inspired by the complex workings of the biological brain. It processes information by simulating the transmission of electrical impulses (spikes) between neurons. The main advantage of SNNs is their bio-interpretability and temporal-dynamic processing, enabling information encoding in precise temporal and spiking patterns, closely approximating the structure and functionality of biological brain. Compared to traditional ANNs, SNNs offer advantages in energy consumption and computational efficiency, particularly in event-driven scenarios. SNN neurons are activated only when receiving or transmitting spikes, resulting in sparse activation and event-driven behavior, making them well-suited for low-power hardware implementations.[175,176] Additionally, mechanisms like rainfall and learning rules for SNNs, including unsupervised spike-time dependent plasticity (STDP) algorithms, enhance their adaptability and learning capabilities. While SNNs may not yet match ANNs accuracy in certain scenarios, their ability to process spatial-temporal information and dynamic visual data, and model neuronal dynamics, positions them as a promising area of AI research.[177-179] Converting ANN models to SNNs retains ANN performance while leveraging SNN efficiency, offering a novel approach for developing more efficient and intelligent computational systems.[180-182]

Han et al. demonstrated configurable NbO_x memristors capable of functioning as either artificial synapses or neurons by controlling the forming compliance current (FCC).[183] When FCC ≤ 2 mA, the device exhibits resistive switching (RS) behavior and multiple forms of synaptic plasticity, including short-term potentiation, paired-pulse facilitation and long-term memory. Conversely, when FCC ≥ 3 mA, the memristor shows threshold switching (TS) characteristics, mimicking neuronal behaviors such as threshold triggering and leaky integrate-and-fire dynamics. By combining RS-type and TS-type NbO_x memristors, a single-layer SNN is simulated and achieved a recognition accuracy of 91% on the MNIST dataset, demonstrating the feasibility of fully memristive neuromorphic systems. In another approach, Palhares et al. explored 28 nm FD-SOI embedded phase-change memories (ePCMs) for cryogenic SNN computing.[184] The Ge-rich $Ge_2Sb_2Te_5$-based ePCM exhibited near-zero resistance drift at 12 K, enabling stable multilevel resistance states for long-term data retention. The simulations reveal that ePCM-based SNNs maintain stable inference accuracy for over 2 years at cryogenic temperatures. These results underscore the potential of ePCMs in brain-inspired cryogenic neuromorphic computing systems. Cheong et al. proposed a neuromodulation-inspired "stashing system" using a self-rectifying charge-trapping memristor array ($Pt/HfO_2/Nb_2O_5/HfO_2/Ti$) to enhance the energy efficiency in SNN learning.[185] In this system, well-trained neurons are temporarily isolated ("stashed") during subsequent training and later reintegrated for inference, mimicking selective neural activation in the biological brain. Hardware demonstrations using a 32 × 32 memristor array validates that the stashing algorithm effectively reduces the energy consumption by 37% without accuracy degradation during MNIST classification. In short, these studies demonstrate that integrating memristive devices with SNN architectures enables tunable, energy-efficient and scalable neuromorphic computation. Through material innovation and bio-inspired system design, SNN hardware could continue to evolve toward brain-like adaptability and cognitive functionality.

Sensing

The rise of smart technologies has significantly increased the demand for sensors in smart systems. Conventional sensors convert data into binary signals that computers can interpret for further processing and analysis. This process detects external information and relies on microprocessors and circuit processing.[186] Recent research on integrated neuromorphic chips has led to a new generation of sensors with the reduced power consumption and enhanced device integration. Researchers are interested in the integrated synaptic sensors, which feature unique mechanisms, including tactile and visual sensors.[187] These sensors form the perceptual foundation of intelligent systems. Tactile sensors simulate human touch and collect information on the shape, texture and pressure of objects, which are crucial for the accuracy and reliability of smart devices. Optical sensors acquire image data about the environment, typically described in terms of image resolution. The captured image is then compared with a baseline image stored in memory for detailed analysis. This section provides an overview of recent research on integrated array of synaptic sensors, focusing on tactile and visual sensors, which explores the potential of these sensors in advancing intelligent systems.[188,189]

Tactile sensors and electronic skin. The skin is the largest sensory organ in the human body, responsible for detecting external stimuli and transmitting electrical signals to the nervous system. Emulating this functionality, integrated synaptic devices have significantly advanced tactile sensor technology by bridging the gap between sensing and processing. With the advancement of AI and the Internet of Things (IoT), the demand for tactile sensing has evolved from simple pressure detection towards high flexibility, multifunctionality and extensive integration, leading to the development of electronic skin (E-skin).

Early research focused on discrete artificial sensory neuron systems to achieve basic tactile processing. For instance, Ye et al. introduced a lead-free $AgBiI_4$ chalcogenide-based artificial synaptic device coupled with a pressure-sensitive film.[190] This system converts mechanical pressure into electrical signals, regulating the synaptic resistance to perform information preprocessing, such as contrast enhancement and noise reduction, thereby improving image recognition accuracy in subsequent neural networks.

As devices evolve toward integrated E-skin, the focus has shifted to mimicking the comprehensive sensory and learning functions of human skin. Lee et al. developed an artificial tactile learning ferroelectric skin (ATFES) based on a ferroelectric field-effect transistor (Fe-FET) with a dome-shaped tactile gate. This device utilizes the polarization flip of P(VDF-TrFE) to emulate synaptic plasticity, enabling the simultaneous detection and learning of pressure patterns with high recognition accuracy even under noisy conditions (Figures 6A-C).[36] Similarly, Wang et al. developed an electronic skin based on synaptic devices that enables real-time sensing of varying pressures and textures (Figures 6D-E).[191]

To further enhance the capabilities of E-skin, multimodal and self-powered functionalities have been explored. Yoon et al. investigated a flexible electronic skin based on synaptic devices capable of dual sensing of temperature and pressure.[192] This electronic skin can be used in wearable devices to monitor the physiological state of the human body, such as heart rate and body temperature, in real-time to support healthcare. From Figure 6F, Liu et al. reported a self-powered synaptic transistor actuated by a triboelectric nanogenerator (TENG),[193] which successfully emulated the synaptic functions including the EPSC, STP and LTP. This approach demonstrates the tactile sensing without the need for external power, offering a promising direction for low-power and self-driven E-skins. As shown in Figure 6G, Zhu et al. developed a soft multifunctional neurological E-skin (SMNE) by integrating an intrinsically stretchable synaptic transistor with flexible mechanoreceptors, thermoreceptors and photoreceptors.[194] This system enables the perception and processing of multiple stimuli (force, temperature and light), allowing robots to perform accurate responses to environmental changes. It demonstrates the potential of neuromorphic sensory systems in intelligent robotics.

In summary, the integration of synaptic devices has driven the evolution of tactile sensors from simple pressure detection to multifunctional, self-powered and intelligent E-skin systems, laying a solid foundation for next-generation wearable devices and human-machine interaction.

Vision sensors. The current generation of neuromorphic vision technologies faces significant challenges, including high power consumption and inefficiencies due to the separation of optical perception, processing and

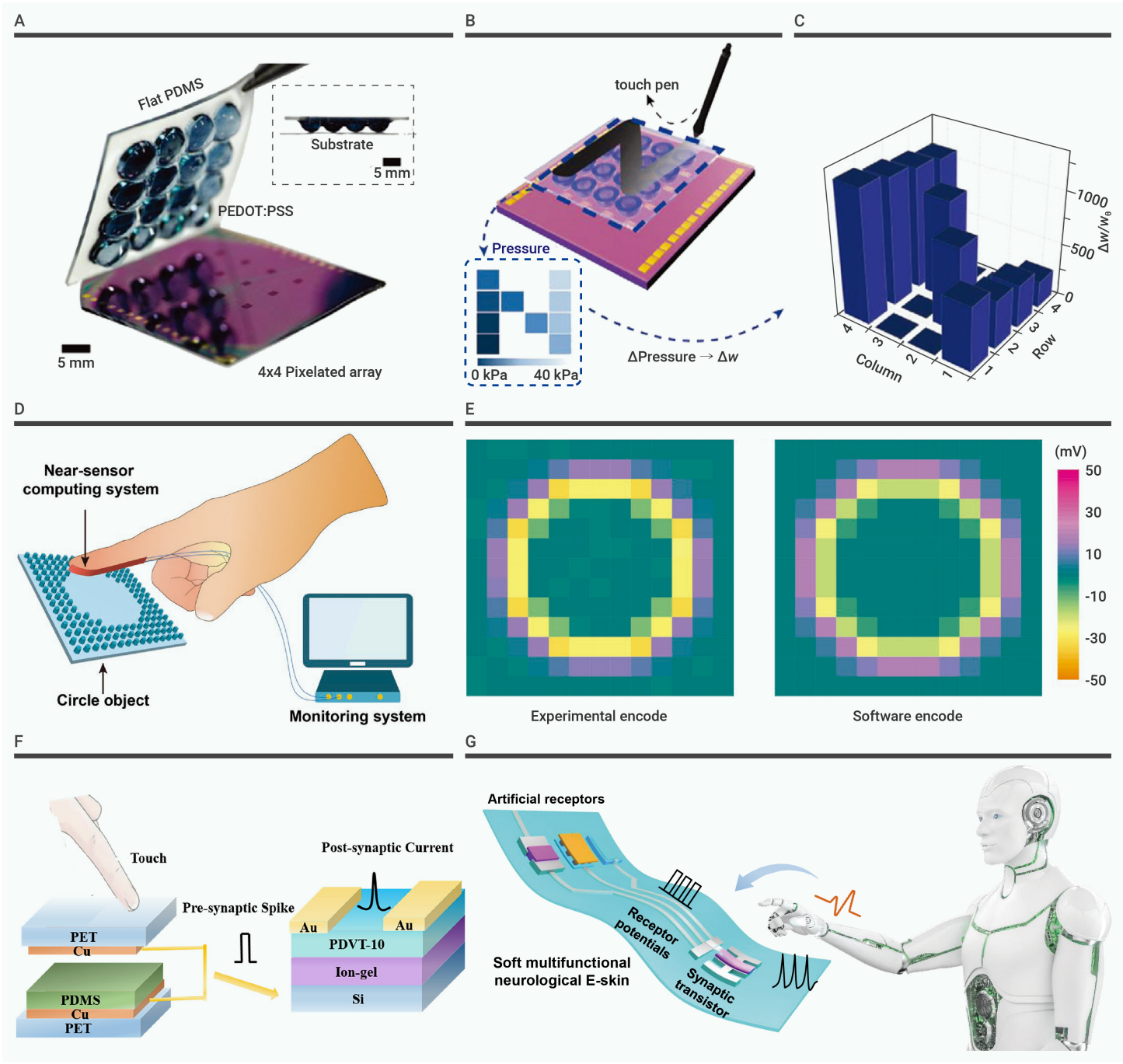


Figure 6. Examples of tactile sensors and electronic skin (A) A photograph of a 4 × 4 pixelated ATFES array combined with dome-shaped PEDOT: PSS gate electrodes positioned on flat PDMS. The inset features a cross-sectional photograph of the ATFES array. (B) A schematic illustration of the alphabet "N" pattern drawn with a commercial touch pen on the 4 × 4 ATFES array. The inset displays the "N" pattern encoded by varying magnitudes of pressure spikes (ranging from 5 × 10^{-2} to 40 kPa) at V_G = -30V. (C) A histogram showing $\Delta w/w_o$ in the 4 × 4 ATFES array. Reproduced with permission.[36] Copyright 2020, Wiley - VCH. (D) Schematic of the experimental setup for edge detection. The flexible near-sensor analogue computing system mounted on the finger is used to scan a circle mold.[191] (E) Edge detection decoded from experiment. Reproduced with permission.[191] Copyright 2022, Wiley - VCH. (F) Schematic representation of an e-skin integrated self-powered tactile synaptic transistor. Reproduced with permission.[193] Copyright 2019, Elsevier. (G) The basic structure of our SMNE. Reproduced with permission.[194] Copyright 2024, Tsinghua University Press.

storage units. To address these limitations, researchers are exploring the development of novel neuromorphic vision systems based on integrated neuromorphic chips. These systems can enhance the computational efficiency and reduce energy consumption by emulating the operational principles of neurons and synapses in the brain. The advent of integrated synaptic arrays has enabled the implementation of numerous synaptic connections on a single neuromorphic chip, essential for constructing complex neural networks and enhancing information processing capabilities. Furthermore, the neuromorphic chip offer high-density integration and parallel processing, both critical for developing advanced computing architectures that combine sensory storage and computation. These technological advancements are expected to lead to more efficient and intelligent information processing in vision sensor technologies.[195-197]

Conventional image sensors in vision systems require transferring data to a memory unit for storage after capturing optical signals. The data is then analyzed and recognized by a processing unit. This process increases system complexity and can result in delays in data transfer and increased energy consumption. In 2024, Jiang et al. proposed the hardware-level image recognition system based on ZnO photoelectric synaptic arrays, which achieves simultaneous sensing and storage of optical signals through its unique photoelectric properties.[198] This optoelectronic synaptic array responds to the changes in light intensity and varies in its responses to the

duration, frequency and number of light stimuli. This functionality mimics the preprocessing capabilities of neurons in the biological retina, such as filtering and noise reduction. As a result, the input data becomes more accurate and efficient for subsequent image processing and recognition tasks. Furthermore, the system incorporates an image denoising function at the hardware level, optimizing the image quality by mapping grayscale values to light stimulus intensity and utilizing the persistent photoconductive effect of the photoelectric synapses for real-time image denoising (Figures 7A-D). The self-denoising function enhances image recognition precision and minimizes the computational resources required in subsequent processing stages, offering a novel approach to more efficient optical neuromorphic computation.

In addition, Zhang et al. introduced an all-optically controlled synaptic device based on an IGZO/SnO/SnS heterostructure.[37] It can mimic the retina-inspired visual sensors and exhibits bidirectional synaptic plasticity under light stimulation. The device exhibits both excitatory and inhibitory synaptic behaviors across a range of UV and visible wavelengths. Additionally, it directly processes optical signals via a simple heterojunction stacking structure and engineered energy bands. Using an ANN simulator, the synaptic device achieves a 91% accuracy in handwritten digit recognition, highlighting its potential for image recognition. Moreover, both the visual imaging and memory processes of the human brain and the damaging effects of UV light on the retinas are simulated using an 8×8 array of photoelectric synapses. As illustrated in Figures 7E–F, the array encodes and recalls characters via sequences of light pulses, thereby simulating both the processes of learning and forgetting visual information. This study offers an insight into the development of all-optically controlled optoelectronic synaptic devices and lays a crucial theoretical and experimental foundation for future sophisticated artificial visual systems.

Integrated neuromorphic chips show significant promise in image recognition and sensing technologies by mimicking the neuronal and synaptic functions of the brain. This capability is evidenced by the enhanced computational efficiency, reduced energy consumption and improved recognition accuracy. These chips manage complex data tasks while providing biological interpretability and dynamic temporal processing, thus paving a new direction for advancing AI systems.

Brain-like computing

As an emerging paradigm, brain-like computing seeks to replicate the neural network structure and information processing mechanisms of the human brain to enable efficient and intelligent computing. In this field, memory effects, particularly in synaptic devices, have become key technologies for brain-like computing due to their unique physical properties.[199,200] Synaptic devices not only replicate the plasticity of biological synapses but also enable the physical integration of data storage and processing, providing robust hardware support for brain-like computing.[201] The multi-state electrical behavior of synaptic device allows the processing and storage of multi-state information, overcoming the limitations of traditional binary logic and enhancing the information processing capabilities of brain-like computation. In specific applications, memory effects are widely used to construct artificial synapses and neural networks. Large-scale synapse arrays enable neuromorphic computation, thereby improving computational efficiency and information processing capacity.[202,203] For example, constructing cross-arrays of synapses enables neural network simulations, thereby increasing computational speed and accuracy.

James et al. introduced an integrated processor chip combining memory arrays and CMOS devices for neuromorphic computing and machine learning. This chip efficiently performs multiply-and-accumulate (MAC) operations, a key step in neural network computation, by integrating a memristor array with CMOS circuitry. The integrated design allows the chip to significantly improve computational efficiency while reducing energy consumption. This design not only demonstrates the potential of memory in neuromorphic computing but also offers a direction for future high-performance, low-power AI hardware.[204] As shown in Figure 8A, Yuan et al. investigated the thermal stability of 1 Mbit RRAM arrays and proposed a high-density 1Mb embedded RRAM macro layout. They enhanced the thermal stability and integration density of the memristor array by optimizing the material and device design. This high-density layout not only improves the performance of memory arrays but also reduces fabrication costs, enabling large-scale commercial applications. Their research provides crucial technical support for the application of memristors in brain-like computing.[205] Moreover, Cai et al. developed a fully integrated, reprogrammable memory/CMOS system for efficient multiplication and accumulation operations. This system achieves efficient neuromorphic computation by integrating the memristor with CMOS circuits (Figure 8B). The integrated design not only improves computational efficiency but also reduces the energy consumption.[206]

In addition, Gao et al. developed a hidden physical unclonable function (PUF) chip using an integrated memristor array and peripheral devices, achieving a zero-bit error rate (BER) and significant resistance to attacks (Figure 8C).[207] This chip provides a highly secure cryptographic function by exploiting the physical properties of the memristor. The non-clonability and high stability of the memory make this chip exceptional in terms of security and reliability, opening new possibilities for the application of brain-like computing in security. Harabi et al. developed a Bayesian machine based on a memristor, capable of performing tasks with localized storage and data (Figure 8D).[208] This machine combines the advantages of a Bayesian network and a memristor to enable efficient probabilistic reasoning and decision-making. This design not only improves computational efficiency but also offers a new insight for future high-performance, low-power brain-like chips.

Overall speaking, the application of integrated neuromorphic chips in brain-like computing holds significant potential. Through interdisciplinary research and collaboration, their performance and applications can be further optimized, advancing the development of brain-like computing. The applications in brain-like computing will continue to expand, offering new possibilities for achieving efficient and intelligent computing.

Intelligent robots

Brain-like chips enable robots to mimic human-like cognitive and learning capabilities by simulating the neural network and neuronal behavior of the human brain. In robotics, brain-like chips primarily contribute to cognitive learning, multimodal information processing and bionic control. Figure 9 illustrates the application of brain-like devices in robotics and highlights their potential in cognitive learning, multimodal information processing and bionic control. For example, a Battenberg vehicle model based on memristor achieves precise control over vehicle behavior by adjusting the conductivity of the memristor array through a supervised learning algorithm, allowing it to accurately follow a predetermined path.[209] On the other hand, a path-planning robot achieves autonomous navigation and path planning in a 2D maze using reinforcement learning.[210] Additionally, brain-like chip-based memristor can switch from short-term to long-term memory, as demonstrated by the memristor-based artificial neural pathway (ANP). It enables rapid response and memory to light signals through repeated electrical stimulation training, allowing the robot to adapt to various task requirements (Figure 9A).[211] In multimodal information processing, the multi-modulation mechanism and structures of brain-like chips enable simultaneous processing of sensory and spatiotemporal information. For instance, a multifunctional optoelectronic hybrid integrated neuron (AOHN) based on memristor integrates spatial and temporal optoelectronic information simultaneously, enabling perception and response to complex environments (Figure 9B).[212] Brain-like chips achieve massively parallel computation through memristor arrays and frequency division multiplexing techniques, such as the parallel processing and classification of image batches via the memristor cross-array structure, improving the information processing speed and efficiency.[213]

In bionic control, brain-like-chip-based neuromorphic circuits mimic the functions of biological neuromuscular junctions (NMJs), which combine analog and digital control advantages. For example, memristor-based neuromuscular junction simulation systems directly control MEMS actuators via ultrasonic distance sensing, enabling precise control of eye movements.[214] Hybrid analog-digital computing platforms based on memristor demonstrate the low latency and high energy efficiency in adaptive balancing robots (Figure 9C), enabling more precise and efficient motion control in complex environments.[215]

In 2025, self-driven memristor synapses based on Ga_2O_3 nanowires were demonstrated to own the considerable potential for humanoid robot learning.[216] These devices can emulate the key biological synaptic functions,

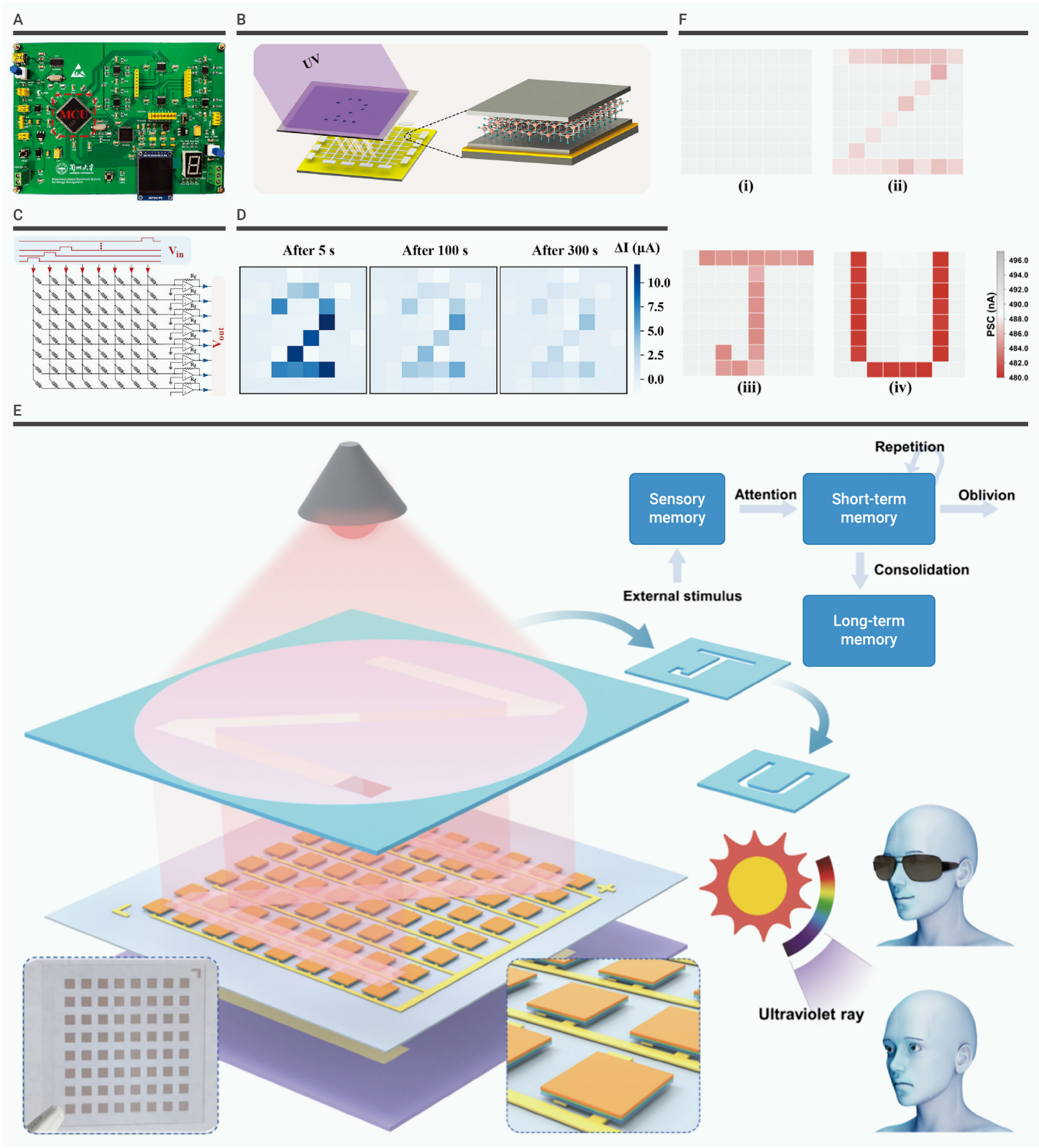


Figure 7. A hardware-level image recognition system based on a ZnO photo-synapse array (A) A hardware test board designated for the image recognition system. (B) A schematic representation of the mapping process from the optical mask pattern to the ZnO photo-synapse array. (C) A circuit diagram illustrating the implementation of current acquisition within the ZnO photo-synapses crossbar array. (D) Image storage characteristics of the ZnO photo-synapse array, where the current matrix is extracted after 5 s (left panel), 100 s (middle panel), and 300 s (right panel) following 10 consecutive pulse stimuli (pulse width: 1 s, pulse interval: 1 s, light intensity: 0.5 mW cm^{-2}). The read voltage is maintained at 1.2 V, and Δ*I* indicates the difference between the photocurrent and the initial dark current. Reproduced with permission.[198] Copyright 2024, Wiley - VCH. A simulation of visual imaging and memory functions in human brain employing the IGZO/SnO/SnS synaptic device array. (E) A schematic illustrating the structure of the IGZO/SnO/SnS synaptic device array alongside the memory formation process akin to human brain function. (F) Illustrations depict the imaging and memory functions for the characters "Z", "J", and "U" at a light wavelength of 658 nm. Reproduced with permission.[37] Copyright 2024, American Chemical Society.

including peak-time–dependent plasticity, impulse facilitation and memory learning. In the experiments, Zhang et al. enabled humanoid robots to execute motor actions such as arm lifting and waving in response to distinct light pulse inputs (Figure 9D), indicating that brain-inspired devices can

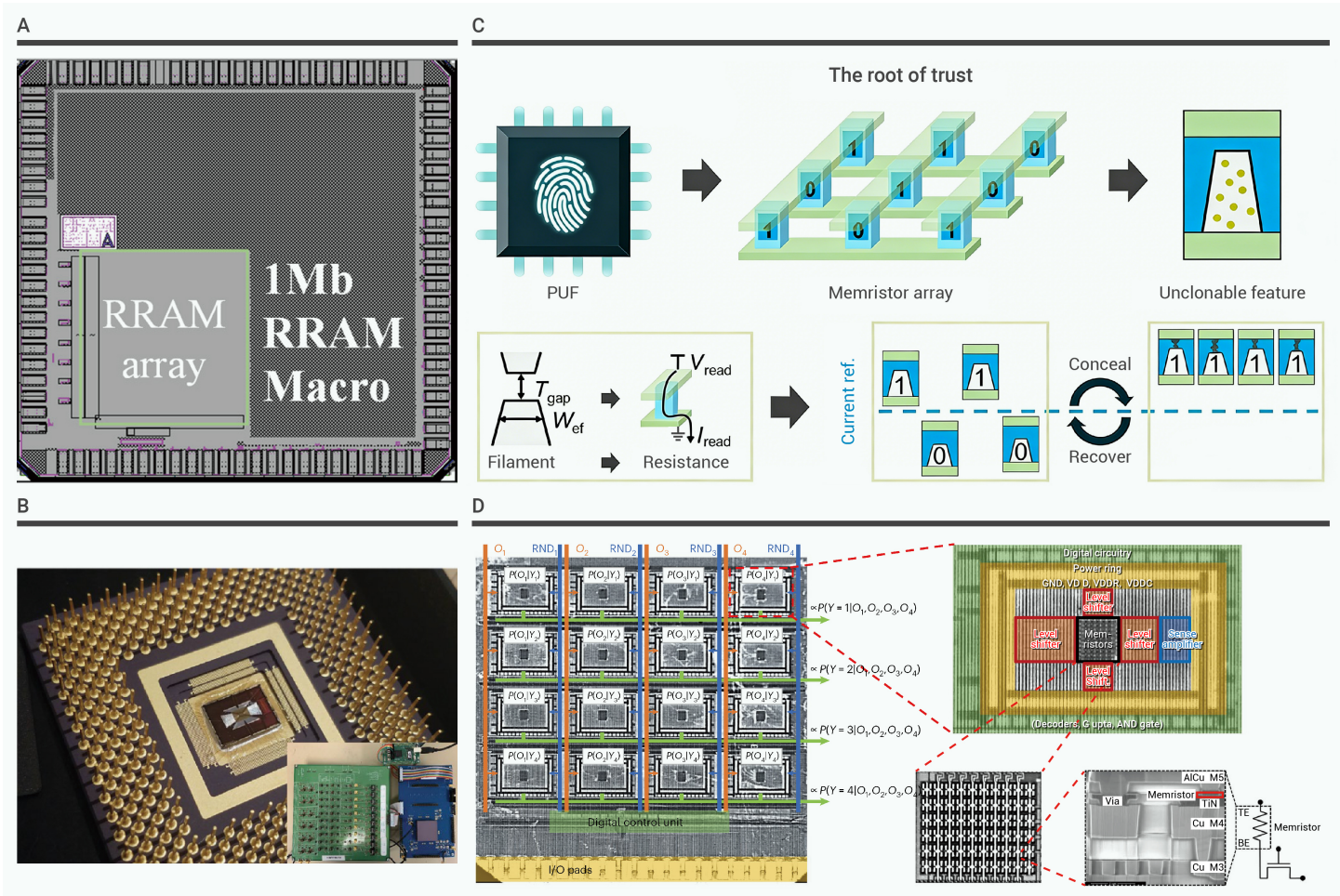


Figure 8. Examples of brain-inspired computing (A) Layout of 1Mb embedded RRAM macro. Reproduced with permission.[205] Copyright 2022, MDPI. (B) Integrated chip wire-bonded on a pin-grid array package. Inset, testing set-up used to power and test the integrated memristor/CMOS chip. Reproduced with permission.[206] Copyright 2019, Springer Nature. (C) The function and mechanism of PUFs for hardware security. PUFs generate unique electronic fingerprints for device identification and data encryption. Furthermore, programming memristors enables effective data concealment and recovery, thereby enhancing security. Reproduced with permission.[207] Copyright 2022, American Association for the Advancement of Science. (D) Optical micrograph of the Bayesian system. Details of the likelihood block, which includes digital circuitry and a memory block with its peripheral circuitry. Micrograph of the 2T2R memristor array. Scanning electron micrograph (SEM) of a memristor in the back-end of the hybrid memristor/CMOS process. Reproduced with permission. Reproduced with permission.[208] Copyright 2022, Springer Nature.

extend beyond cognitive learning to the direct control of motor behavior.[216] Building on this concept, they further developed a graphene/(Al,Ga)N nanowire–based dual-mode synaptic device that further illustrates the promise of synaptic electronics in robotics (Figure 9E).[217] Operating as a self-powered UV photodetector under zero bias and as an ultralow-energy artificial synapse under external bias, the device supports the learning–forgetting–relearning cycles. When integrated into humanoid robots, these dual-mode devices enable the real-time light-direction sensing and adaptive motor control, including orientation adjustment and memory-guided actions.

Beyond basic motion execution, deeply integrating neuromorphic chips into the robot perception-compute-actuation loop to enable multitasking, autonomous navigation and embodied adaptability represents a key frontier in intelligent robotics. First, mobile robots in complex environments require the capability for low-latency, multimodal multitasking. Ma et al. developed the TianjicX neuromorphic chip, which features a spatiotemporally elastic architecture supporting the asynchronous execution of multiple neural network models.[218] The mobile robot "Tianjicat" built upon this chip, successfully demonstrated the concurrent execution of sound tracking, object recognition, obstacle avoidance and decision-making. Compared to a traditional embedded GPU (NVIDIA Jetson TX2), the system reduced latency by approximately 79-fold and dynamic power consumption by over 50%, demonstrating the immense advantage of dedicated neuromorphic hardware for edge robotic computing. Second, autonomous navigation (e.g., SLAM) and path planning are core manifestations of robotic intelligence. Yang et al. reviewed advancements in neuromorphic electronics for robotic perception and navigation.[219] By utilizing brain-inspired chips to run spiking neural networks (SNNs) coupled with event-based sensors (e.g., DVS), robots can achieve energy-efficient simultaneous localization and mapping (SLAM) in unknown environments. This spike-based sparse computing paradigm significantly reduces data redundancy, making it particularly suitable for resource-constrained micro-robots conducting long-term autonomous exploration. Finally, endowing robots with "Embodied Intelligence" to adapt to dynamic environments is the ultimate goal. Putra et al. proposed the concept of "Embodied Neuromorphic Artificial Intelligence", emphasizing the importance of hardware-software co-design. By leveraging the online learning capabilities of SNNs (e.g., STDP-based unsupervised learning), robots can continuously update their knowledge through interaction with the environment at runtime, thereby adapting to unforeseen changes. This self-adaptive capability, often lacking in traditional pre-programmed robots, marks a transition from automation to true intelligence.

Hence, these advances highlight how synaptic devices can effectively bridge perception and action, extending brain-inspired chips from cognitive processing toward energy-efficient and adaptive motor control in robotic systems. Brain-like chips grant robots human-like intelligence and learning capabilities, allowing them to autonomously adapt and optimize behavior in complex environments. Future research will focus on enhancing the performance of brain-like chips and addressing challenges like device uniformity and weak signal detection to achieve more efficient and intelligent robotic systems.

Neuromorphic computing paradigms and system challenges

In recent years, the rapid development of neuromorphic computing archi-

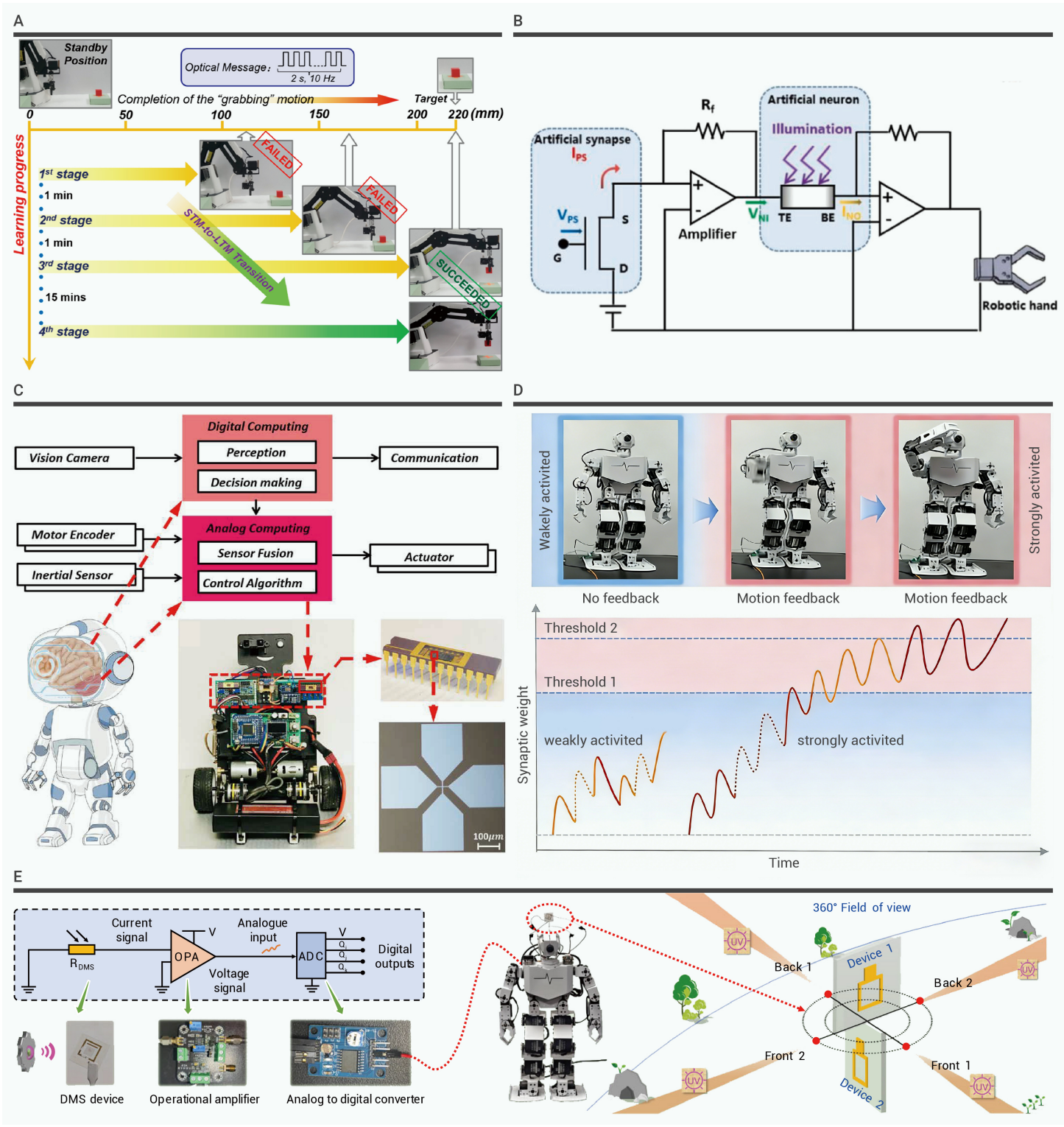


Figure 9. Examples of intelligent robots (A) Optical signals enabled ANP to learn and directly grasp the target after motion improvement and memory recall. Reproduced with permission.[211] Copyright 2022, American Chemical Society. (B) Schematic diagram of circuit implementation in human dynamic training process. Reproduced with permission.[212] Copyright 2022, Elsevier. (C) The hybrid analog-digital computing platform, inspired by brain structure, features an analog component acting as the cerebellum to control robotic motion and a digital component functioning as the cerebrum to execute high-level algorithms. The study also presents images of the mobile robotic system (a mobile inverted pendulum), packaged memristors on a chip carrier, and an optical microscope image of a Pt/Al_2O_3/Ta/Pt cross-point memristor (scale bar: 100 μm). Reproduced with permission.[215] Copyright 2020, American Association for the Advancement of Science. (D) The self-driven memristor synapse generates distinct electrical signals under varying light stimuli to drive the humanoid robot to perform different actions. Reproduced with permission.[216] Copyright 2024, Wiley - VCH. (E) Schematic of the humanoid robot control system incorporating an operational amplifier (OPA) and an analog-to-digital converter (ADC), together with the UV detection configuration using two orthogonally arranged transparent dual-mode devices. Reproduced with permission.[217] Copyright 2025, The Authors, distributed under CC BY 4.0.

tectures has shifted system-level research from device-centric demonstrations toward cross-layer computational frameworks. To provide a more comprehensive discussion of neuromorphic applications, it is essential to analyze these architectures from a system perspective. First, although analog cross-bar arrays offer the potential for highly efficient parallel matrix–vector multiplication (MVM), their practical deployment at large scale is significantly constrained by inherent physical and architectural limitations. These include IR-drop-induced weight distortion, device-to-device variability, nonlinear and

asymmetric conductance updates, sneak-path leakage, limited programming precision, and endurance degradation, all of which deteriorate computational accuracy when scaling from small arrays to chip-level systems.[220-222] These challenges represent major bottlenecks for the practical adoption of analog neuromorphic accelerators.

Meanwhile, fundamental architectural differences have emerged among ANN accelerators, SNN processors and in-sensor computing architectures. ANN accelerators rely on digital or analog MAC operations and benefit from a mature training ecosystem, yet their energy consumption is dominated by data movement. SNN processors exploit event-driven sparse computation and are well suited for low-power and online-learning tasks, though their training remains nontrivial.[223,224] In contrast, in-sensor computing, which tightly integrates sensing and computation, fundamentally suppresses the data-movement bottleneck. Recent optoelectronic synapse-based vision front-end chips have demonstrated superior performance in image classification, dynamic vision processing and noise suppression.[102,225] Therefore, these complementary computing paradigms form the major technological pathways driving neuromorphic system development.

Alongside architectural advances, several representative neuromorphic chips have demonstrated the feasibility of system-level neuromorphic intelligence. IBM TrueNorth incorporates one million neurons and 2.56×10^8 synapses, enabling milliwatt-level inference.[226] Intel Loihi and Loihi 2 support diverse synaptic plasticity mechanisms such as STDP and three-factor learning, enabling adaptive, low-power intelligent computation.[224] The TianjiC and TianjicX processors further integrate hybrid ANN–SNN computing architectures and have been validated in intelligent decision-making tasks.[20,218] These platforms collectively indicate that neuromorphic computing is transitioning from device-level concepts to practical system-level implementations. Future progress will rely on co-design across device, circuit, architecture, algorithm and application layers to achieve high energy efficiency, low latency, and scalable neuromorphic intelligence.

Potential applications

The integrated neuromorphic chips, utilizing the neuromorphic computing capabilities of synaptic devices, have powerful sensing and processing capabilities that enable real-time, highly sensitive sensing. Its multimodal sensing capability opens broad application prospects across various fields. Its application in healthcare is promising.[227,228] As shown in Figure 10A, first, the integrated neuromorphic chips can be incorporated into wearable health monitoring devices to monitor the physiological state of the body in real time, such as heart rate, body temperature and blood pressure. These devices can enable telemedicine and personalized health management, helping doctors adjust treatment plans promptly. Second, they can also be used in rehabilitation to help patients restore sensory and motor functions. For example, integrating them into rehabilitation equipment allows haptic feedback to aid patients in rehabilitation training. Lastly, neuromorphic chips can be integrated into smart prostheses to provide haptic feedback, making them more akin to natural limbs and significantly improving the quality of life for amputee patients.

In human-computer interaction and brain-computer interface, the integrated neuromorphic chips can also have significant application potential. They are used in virtual reality and augmented reality devices to provide haptic feedback, enhancing the user's immersion and interaction experience. For example, users can feel the texture and temperature of objects in a virtual environment, improving the realism. Then, it can be integrated into smart wearable devices to provide real-time environmental sensing and health monitoring. For example, smartwatches can use neuromorphic chips to sense temperature and pressure, providing real-time environmental data. Moreover, integrated neuromorphic chips can be used in smart homes and buildings to sense physical stimuli such as temperature, humidity and pressure, enabling smarter home control and building management.

The integration of synaptic memristive devices into brain–computer interfaces (BCIs) have evolved from neural signal analysis to adaptive closed-loop control. Liu et al. demonstrated a memristor-array-based neural signal analysis system that efficiently filtered and identified epilepsy-related brain activities with over 400 times higher energy efficiency than CMOS circuits.[229] In Figure 10B, Dias et al. developed a memristor-based neuromodulation interface capable of real-time monitoring and adaptive control of neuronal populations, where the device acted as an artificial synapse with reversible short-term plasticity.[38] Furthermore, Liu et al. realized a large-scale 128 k-cell memristor chip as an adaptive neuromorphic decoder for real-time drone control, achieving software-equivalent accuracy with ultra-low power consumption and demonstrating brain–memristor co-evolution.[80] Hence, these works highlight that integrating synaptic devices into BCIs enables low-latency, bioinspired and self-adaptive interfaces for next-generation neuroprosthetic and immersive human–machine interaction systems.

In addition, integrated neuromorphic chips have significant potential in intelligent robotics. They can be used in the skin of humanoid robots to enable them to sense environmental stimuli, such as pressure, temperature and texture. This will help robots better adapt to complex environments, allowing for more natural and flexible interactions. Furthermore, they can be used in service robots to sense and respond to users' tactile inputs, offering more personalized services. For example, service robots can use neuromorphic chips to sense user touch, offering a more natural interaction experience. In Figure 10C, Bao et al. demonstrated a 3D-printed humanoid hand integrating Kresling-origami pressure sensors with a synaptic transistor–based neuromorphic circuit, allowing adaptive grasping of unknown objects without external controllers. The system autonomously enhances its grip through repetitive training, emulating human spinal reflex learning. It employs six-axis robot-assisted direct ink writing for printing conductive traces on complex 3D surfaces, which provides a scalable approach for flexible, high-density and bio-inspired robotic platforms.[230] In industrial robots, neuromorphic chips improve the operational precision and efficiency, particularly in scenarios requiring high sensitivity and real-time response.

In the field of aerial vehicles, neuromorphic chips have demonstrated unique advantages in real-time perception, efficient control and adaptability to extreme environments. Conventional unmanned aerial vehicles (UAVs) often rely on power-hungry GPUs or embedded processors, limiting their miniaturization and response speed, particularly in resource-constrained micro-aircraft. As shown in Figure 10D, Paredes-Vallés et al. developed a fully neuromorphic vision–control integrated system that achieves end-to-end flight control based on event-camera inputs.[231] By deploying a spiking neural network (SNN) on the Intel Loihi neuromorphic chip, the quadrotor system performs visual perception and control command generation at 200 Hz with only 7–12 mW of power consumption, significantly lower than traditional embedded GPU platforms. The vision module extracts optical flow from raw event streams through self-supervised learning, while the control module employs an evolution-trained linear decoder to execute hovering, landing and lateral maneuvers, showing strong sim-to-real transferability. This work verifies the feasibility of neuromorphic hardware for autonomous flight control, providing a low-power, adaptive pathway toward insect-scale micro-air vehicles, deep-space exploration drones, and swarm-intelligent flight systems capable of GPS-free navigation in complex and dynamic environments.

SUMMARY AND OUTLOOK

This review has provided a comprehensive overview of recent progress in integrated neuromorphic chips, spanning from fundamental memristive mechanisms and diverse material-structure configurations to advanced heterogeneous integration technologies and their transformative applications. While significant breakthroughs have been achieved, bridging the gap from laboratory prototypes to large-scale practical deployment requires addressing critical bottlenecks across three hierarchical levels.

At the device level, the primary challenge lies in reconciling the intrinsic trade-offs between linearity, dynamic range and reliability within a single synaptic element. Although novel materials such as metal oxides and 2D materials have demonstrated promising scalability, the stochastic nature of ion migration inevitably leads to cycle-to-cycle and device-to-device variability, which introduces noise that degrades the precision of neural inference. Furthermore, achieving linear and symmetric weight updates remains difficult in filamentary switching mechanisms, and limited endurance under high-frequency operation continues to hinder commercial adoption. Future research therefore prioritizes interface engineering and defect control to minimize stochasticity while exploring non-volatile mechanisms that offer both high switching speed and robust analog retention.

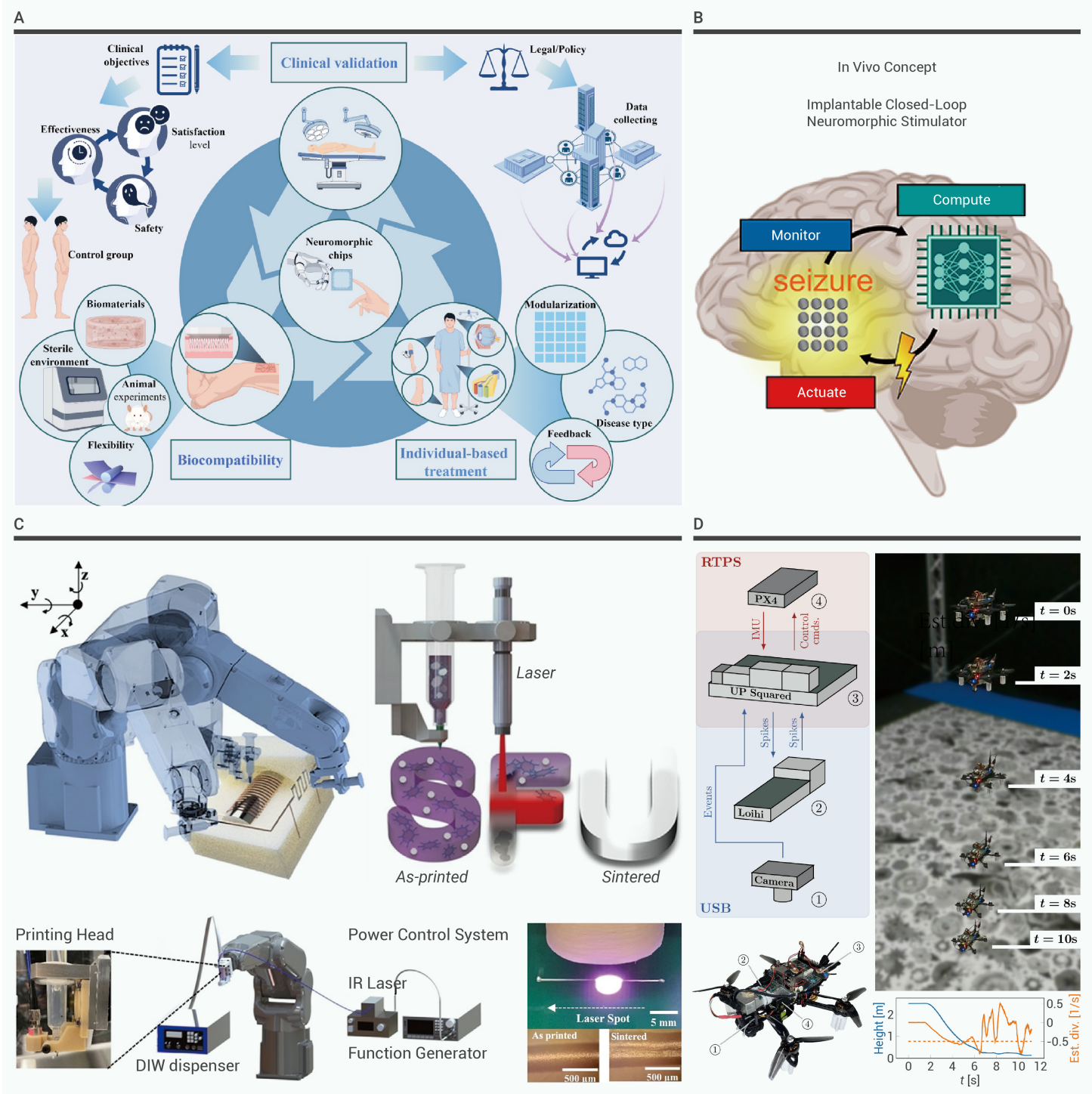


Figure 10. Examples of potential applications (A) The research line of neuromorphic chips in the field of biomedical engineering includes three aspects: biocompatibility, individual-based treatment and clinical validation. Reproduced with permission.[228] Copyright 2025, Elsevier. (B) The proposed in vivo concept of neuromodulation device. Reproduced with permission.[38] Copyright 2022, American Chemical Society. (C) Schematic diagram of robot 3D printing for three different types of surfaces. Schematic diagram of printing procedure with in situ laser sintering. The six-axis robot 3D printing setup. Reproduced with permission.[230] Copyright 2022, The Authors, distributed under CC BY 4.0. (D) Hardware overview shows the communication among event camera, neuromorphic processor, single-board computer, and flight controller. Composite picture and graph demonstrating the system for an optical flow constant divergence landing, with estimated divergence (solid orange line) oscillating around a set point (dashed orange line) while height is decreasing (solid blue line). Reproduced with permission.[231] Copyright 2024, American Association for the Advancement of Science.

At the circuit level, scaling up from discrete devices to massive crossbar arrays introduces dominant physical constraints related to parasites and interconnects. A critical bottleneck is the parasitic resistance in large-scale analog arrays, which causes significant voltage drops (IR drop) along word and bit lines. This effect leads to deviations in the effective voltage applied to memory cells, resulting in severe computational errors that are spatially dependent and difficult to compensate for mathematically. Additionally, as the integration density increases, the "memory wall" becomes more pronounced, necessitating advanced solutions such as 3D heterogeneous integration and processing-in-memory (PIM) architectures to minimize the energy latency of data movement. Circuit designers need to tackle the integration of area-efficient peripheral interfaces (e.g., ADCs/DACs) and implement robust selector technologies to suppress sneak path currents in high-density arrays.

At the system level, relying solely on device or circuit improvements is insufficient to meet the demands of complex intelligent tasks, necessitating a

paradigm shift toward algorithm–hardware co-design. Future systems should move beyond agnostic algorithms to adopt "fault-aware" training strategies that can proactively tolerate and adapt to hardware imperfections such as variability and stuck-at faults. Moreover, to support the dynamic mapping of diverse neural network models (ANNs, SNNs and hybrids) onto physical hardware, architectural elasticity is essential. Developing comprehensive compiler stacks that can automatically optimize spatiotemporal resource allocation, which will be the key to bridging the gap between abstract algorithmic models and non-ideal physical hardware, ultimately enabling robust, adaptive and energy-efficient neuromorphic intelligence.

In conclusion, the advancement of integrated neuromorphic chips constitutes a critical evolution in computing architecture, necessitating the synergistic integration of materials science, circuit design and algorithm optimization. Bridging the current gaps in device stability, array scalability and system compatibility is essential for translating these bio-inspired prototypes into practical hardware. As these interdisciplinary challenges are addressed, neuromorphic chips are expected to provide the energy-efficient computational foundation necessary for next-generation autonomous robotics, healthcare monitoring and human-machine interfaces in the post-Moore era.

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AUTHOR CONTRIBUTIONS

Y.K.Z. conceived the idea. Y.K.Z., L.F.B., C.Y.S., and J.Y.Z. guided the work. X.S.G., Y.K.Z. and L.F.B. wrote the original draft of this review. Y.K.Z., L.F.B. and J.Y.Z. carried out the funding acquisition and project administration. X.S.G., L.R.C., Y.B.W. and C.Y.S. carried out the visualization of this work. X.S.G., L.R.C. and Y.B.W. performed the investigation. All authors reviewed this manuscript. All authors contributed to the manuscript and approved the final version.

DECLARATION OF INTERESTS

The authors declare no competing interests.

ETHICAL STATEMENT AND PATIENT CONSENT

Not Applicable.

DATA AND CODE AVAILABILITY

No new data were created or analyzed in this study.